

Additional improvements in the invention have centered in the modulator algorithm. For the 'odd-m' frequency and 'in-phase' timing configurations shown in FIG. 5, there are two ways to generate the appropriate digital code. The first uses any standard modulator algorithm (typically a second order delta-sigma modulator.) The second is a simple but very important modification to the modulator that increases the signal to noise ratio by decreasing the in-band harmonics of the quantization noise.

The first method uses a standard modulator that generates three output levels (Low, Middle, and High.) Then, a three-level to two-level transformation is added to the modulator's finished three-level code, so that the code can be implemented using the two-level code generator. In the transformation Low corresponds to two consecutive bits 00, middle corresponds to 01 and high corresponds to 11. Choosing 01 for the middle level fixes the relative phase between the code and sine wave so that the in-phase condition can apply to all bits. This technique successfully increases the operating margins for the code, but at the same time it decreases the signal-to noise ratio by increasing the in-band harmonics compared to the untransformed three-level modulator code. This results because the modulator cannot optimize the code at each 0 or 1 bit for the two-level operation.

The second method solves this problem by including the relative phase choice within the feedback loop of a two-level modulator algorithm. The in-phase condition requires that the code contain only odd numbers of consecutive identical bits, for example, three 1's and one 0, etc. Every two-level modulator has a comparator that determines whether the next bit is a 1 (signal is positive) or 0 (signal is negative.) The modified modulator of this invention allows the comparator to change the polarity of the next bit only if there is an odd number of previous consecutive bits of the same polarity. This restriction forces the code to have an odd number of consecutive bits of the same polarity. As a result, the new modulator directly generates two-level codes appropriate for the optimum in-phase condition and for improved operating margins. Since the restricted comparator is inside the feedback loop of the modulator, it improves signal-to-noise ratio compared to the first method.

Neither of these two methods for generating the code give signal to noise ratios as low as the standard two-level modulator, but they are essential for achieving the larger output voltages that are the main limitation for many useful Josephson applications. The large oversampling ratios that can be used for the metrology application yield significantly large signal-to-noise ratios so that signal-to-noise can be sacrificed for larger operating margins and output voltage.

While the invention has been shown and described with reference to preferred embodiments thereof, it should be understood that changes in the form and details of the invention may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit for producing an electrical signal which is a replication of a mathematical model which can include ac and/or dc bipolar waveforms comprising:

a modulator wherein an output sequence of zeros and ones produced by said modulator represents said mathematical model;

a digital code generator connected to receive said output sequence from said modulator wherein an output digital code signal is produced to represent said mathematical model;

a sinusoidal frequency generator whose output drive frequency is synchronized to said digital code;

a Josephson quantizer connected to be driven by said digital code generator and said frequency generator wherein the quantized bipolar output pulses of said Josephson quantizer represent said mathematical model; and

an analog low pass filter connected to receive said quantized bipolar output pulses and produce an output signal which is a replication of said mathematical model including models of ac and dc bipolar waveforms.

2. The circuit of claim 1 further including

a synchronizing circuit producing a sampling frequency produced  $f_s$ , connected to said digital code generator and to said sinusoidal frequency generator.

3. The circuit of claim 2 wherein the drive frequency produced by said sinusoidal frequency generator is capable of being set to one of half integer multiples of said sampling frequency and equal to  $mf_s/2$  where the integer  $m$  is  $\geq 2$ .

4. The circuit of claim 3 wherein  $m$  is equal to the integer 3.

5. The circuit of claim 3 wherein said modulator is a delta-sigma modulator.

6. The circuit of claim 3 wherein said Josephson quantizer is comprised of at least one Josephson junction.

7. The circuit of claim 6 wherein the maximum peak-to-peak output voltage of said at least one Josephson junction is equal to  $Nmf_s/K_J$  where  $N$  is the number of junctions,  $n$  is the Josephson junction constant voltage step number and is equal to the number of output voltage pulses produced for each input current pulse,  $f_s$  is the sampling frequency and  $K_J$  is the Josephson constant.

8. The circuit of claim 6 wherein said at least one Josephson junction is an Nb—PdAu—Nb junction.

9. The circuit of claim 3 further including a combining circuit connected to receive the output of said digital code generator and the output of said sinusoidal frequency generator and supply a combined signal to said quantizer.

10. The circuit of claim 9 wherein said combining circuit is a directional coupler.

11. The circuit of claim 3 optimized to produce a bipolar voltage standard source operating at maximum output voltage  $V$  at a first Josephson voltage step ( $n=1$ ) according to an optimizing method comprising:

(1) providing the fastest digital code generator available;

(2) providing at least one Josephson junction with a characteristic frequency,  $f_c=1.5f_s$ ;

(3) providing a sinusoidal frequency  $f=1.5f_s$ ;

(4) providing sinusoidal input current amplitude,  $I_{ac}$ , to maximize said  $n=1$  step voltage;

(5) providing for the centering of the Josephson junction current range on the zero current axis at the  $n=+1$  step by adjusting the digital code high level current amplitude when using an all 1's code;

(6) providing for the centering of the Josephson junction current range on the zero current axis at the  $n=-1$  step by adjusting the digital code low level current amplitude when using an all 0's code; and

(7) providing for in-phase operation between the digital code generator and said sinusoidal frequency generator.

12. The circuit of claim 3 wherein the integer  $m$  is an odd integer and wherein said modulator includes a three-level comparator, said circuit further including a transformation algorithm to change the modulator's finished three-level code to a two-level code by having low correspond to 00, middle correspond to 01, and high correspond to 11 to establish in-phase condition between said output sequence and said sine wave.