US006170743B1

(12) **United States Patent**
Okaue et al.

(10) **Patent No.: US 6,170,743 B1**
(45) **Date of Patent: Jan. 9, 2001**

(54) **EXTERNAL STORAGE APPARATUS AND CONTROL APPARATUS THEREOF AND DATA TRANSMISSION/RECEPTION APPARATUS**

(75) Inventors: **Takumi Okaue**, Kanagawa; **Yoshio Kondo**, Chiba, both of (JP)

(73) Assignee: **Sony Corporation**, Tokyo (JP)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/086,788**

(22) Filed: **May 28, 1998**

(30) **Foreign Application Priority Data**

Jun. 4, 1997 (JP) 9-146913

(51) **Int. Cl.**[7] **G06K 5/00**

(52) **U.S. Cl.** **235/380**; 235/492; 235/379; 235/449; 902/25; 902/26

(58) **Field of Search** 235/492, 493, 235/380, 379, 449; 902/25, 26, 27

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,454,414	*	6/1984	Benton	235/379
4,625,276	*	11/1986	Benton et al.	364/408
4,990,760	*	2/1991	Tomari et al.	235/492
5,072,103	*	12/1991	Nara	235/492
5,083,286	*	1/1992	Hino et al.	395/115
5,163,111	*	11/1992	Baji et al.	395/22
5,245,582	*	9/1993	Kimura	365/229
5,267,218	*	11/1993	Elbert	365/226
5,388,248	*	2/1995	Robibson et al.	395/425
5,422,855	*	6/1995	Eslick et al.	365/226
5,428,579	*	6/1995	Robinson et al.	365/230.03
5,504,701	*	4/1996	Takahashi et al.	365/185.04
5,537,584	*	7/1996	Miyai et al.	395/183.18
5,615,388	*	3/1997	Yoshimatsu et al.	395/821
5,678,029	*	10/1997	Iijima	395/500
5,745,912	*	4/1998	Konishi et al.	711/103
5,796,092	*	8/1998	Nagata et al.	235/492
5,974,513	*	10/1999	Matsuo et al.	711/164

FOREIGN PATENT DOCUMENTS

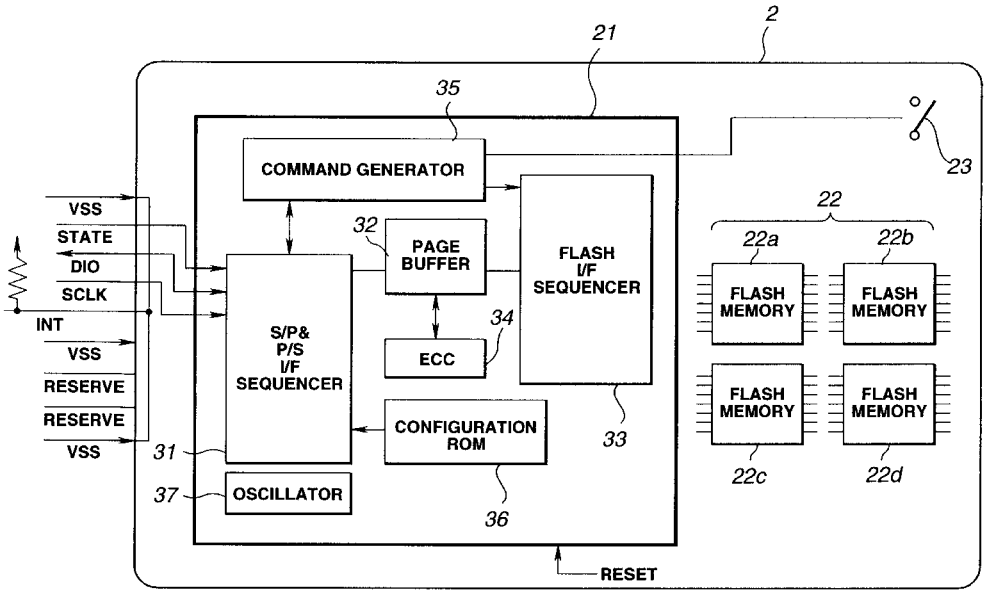
62-48097	3/1987	(JP) .
62-179037	8/1987	(JP) .
3-124397	12/1991	(JP) .
5-047189	2/1993	(JP) .
5-173888	7/1993	(JP) .
10-171938	6/1998	(JP) .

* cited by examiner

Primary Examiner—David V. Bruce
Assistant Examiner—Daniel S Felten
(74) *Attorney, Agent, or Firm*—Frommer Lawrence & Haug, LLP; William S. Frommer

(57) **ABSTRACT**

The object of the present invention is to enable to prevent an erroneous erase of a data stored or writing another data on the data as well as to enable to easily switch an erroneous erase prevention switch.

A command generator, upon reception of a register instruction for checking a state of a memory card received via an S/P & P/S sequencer, sets a state of an erroneous erase prevention switch in a register and transmits this register content via the S/P & P/S sequencer to a host computer. According to the register content from the memory card, the host computer decides whether a write protect is ON and executes a write inhibit processing when the write protect is ON.

12 Claims, 6 Drawing Sheets