

I claim:

- 1. A logic state analyzer for producing a symbolically annotated trace listing of selected logic states occurring during a target system's execution of a relocated machine code object program that was produced from a source program incorporating symbolic labels, and was linked and loaded, the logic state analyzer comprising:
  - correspondence means, coupled to files associated with the linking and loading of the machine code object program, for producing a table of correspondence between symbolic labels used in the source program and corresponding absolute addresses within the relocated machine code object program that occur as states in the target system;
  - trace specification means, coupled to the correspondence means, for specifying in terms of the symbolic labels a condition to be met by a logic state occurring in the target system in order for that logic state to be included in the selected trace;
  - logic state acquisition means, coupled to the trace specification means, for coupling to the target system and acquiring the values of logic states that occur therein and satisfy the condition specified by the trace specification means;
  - memory means, coupled to the logic state acquisition means, for storing numerically the values of the logic states acquired by the logic state acquisition means;
  - conversion means, coupled to the correspondence means and to the memory means, for converting from numerical values into their associated symbolic labels those acquired logic state values stored in the memory means which have associated symbolic labels in the table of correspondence produced by the correspondence means; and
  - output means coupled to the conversion means for producing an indication of the numerical values and symbolic labels of the logic states included in the trace.
- 2. A logic state analyzer as in claim 1 wherein the output means is additionally responsive to the source program from which the object program was produced, and wherein the indication produced by the output means includes, interspersed with portions of the numeric values and symbolic labels of the logic states included in the trace, those individual source program lines whose associated machine code object program execution resulted in the aforesaid portions.
- 3. A logic state analyzer as in claim 1 wherein the source program is compiled by a compiler and at least one correspondence in the table of correspondence pertains to a symbolic label appearing in a symbol table produced by that compiler.
- 4. A logic state analyzer as in claim 1 wherein the source program is assembled by an assembler and at least one correspondence in the table of correspondence pertains to a symbolic label appearing in a symbol table produced by that assembler.
- 5. A logic state analyzer as in claim 1 wherein at least one correspondence in the table of correspondence is supplied by the user of the logic state analyzer and associates the numerical value of a selected logic state in the target system with an auxiliary symbolic label chosen by the user to represent that selected logic state.
- 6. A logic state analyzer as in claim 1 wherein the indication produced by the output means comprises a visible indication.
- 7. A logic state analyzer as in claim 1 wherein the

- target system includes a memory management unit, coupled to the correspondence means, that dynamically alters correspondence between virtual addresses and physical addresses of a target system memory, and wherein the correspondence means is responsive to the dynamic alterations of the memory management unit by offsetting the absolute address associated with each symbolic label by an amount corresponding to each alteration in the correspondence between virtual and physical address.
- 8. A logic state analyzer as in claim 1 wherein at least one entry in the table of correspondence associates a symbolic label with a range of absolute addresses.
- 9. A logic state analyzer as in claim 8 wherein the conversion means converts a numerical value falling within the range of absolute addresses associated with a symbolic label into an offset relative to a selected value in that range and wherein the indication produced by the output means comprises that symbolic label and that offset.
- 10. A logic state analyzer for producing a symbolically annotated trace listing of selected logic state values occurring during the operation of a target system, the logic state analyzer comprising:
  - correspondence means, responsive to the user of the logic state analyzer, for producing a table of correspondence between logic state values that occur during the operation of the target system and symbolic labels chosen by the user to represent those logic state values in lieu of their numeric representation;
  - trace specification means, coupled to the correspondence means, for specifying in terms of the symbolic labels a condition to be met by a logic state value occurring in the target system in order for that logic state value to be included in the selected trace;
  - logic state acquisition means, coupled to the trace specification means, for coupling to the target system and acquiring the values of logic states that occur therein and satisfy the condition specified by the trace specification means;
  - memory means, coupled to the logic state acquisition means, for storing numerically the values of the logic states acquired by the logic state acquisition means;
  - conversion means, coupled to the correspondence means and to the memory means, for converting from numerical values into their associated symbolic labels those acquired logic state values stored in the memory means which have associated symbolic labels in the table of correspondence produced by the correspondence means; and
  - output means coupled to the conversion means for producing an indication of the numerical values and symbolic labels of the logic states included in the trace.
- 11. A logic state analyzer as in claim 10 wherein at least one entry in the table of correspondence associates a symbolic label with a range of logic state values.
- 12. A logic state analyzer as in claim 10 wherein the conversion means converts a numerical value falling within the range of logic state values associated with a symbolic label into an offset relative to a selected value in that range and wherein the indication produced by the output means comprises that symbolic label and that offset.

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