

[54] LOGIC ANALYZER USING SOURCE PROGRAM OR OTHER USER DEFINED SYMBOLS IN THE TRACE SPECIFICATION AND THE TRACE LISTING

[75] Inventor: Bryce S. Goodwin, Jr., Colorado Springs, Colo.

[73] Assignee: Hewlett-Packard Company, Palo Alto, Calif.

[21] Appl. No.: 814,013

[22] Filed: Dec. 20, 1985

Related U.S. Application Data

[63] Continuation of Ser. No. 481,010, Mar. 31, 1983, abandoned.

[51] Int. Cl.⁴ G06F 11/34

[52] U.S. Cl. 364/200; 371/19

[58] Field of Search 364/200, 900, 486, 580; 324/73 R, 73 AT; 371/17, 19

[56] References Cited

U.S. PATENT DOCUMENTS

4,099,230	7/1978	Mead	364/200
4,205,370	5/1980	Hirtle	364/200
4,250,262	2/1981	Haag et al.	364/900
4,381,563	4/1983	Groom, Jr. et al.	324/73 R
4,434,488	2/1984	Palmquist et al.	324/73 R
4,533,997	8/1985	Ferguson	364/200

Primary Examiner—James D. Thomas
 Assistant Examiner—David L. Clark
 Attorney, Agent, or Firm—Edward L. Miller

[57] ABSTRACT

A logic state analyzer allows a user to include symbols

defined in source program listings, as well as other specially defined symbols, in the trace specification. Such symbols represent unique individual values or ranges of values. The resulting trace list includes these symbols, and where possible, all address, operands, etc., are expressed in such terms. When those symbols are relocatable entities produced by compilers and assemblers the result is that the user is freed from having to duplicate the relocation process to specify absolute values in the trace specification, and later reverse it to interpret absolute values in the listing in terms of symbols originally defined in the source programming. A further result is that the states within an arbitrary finite state machine can be assigned descriptive labels, with the trace specification and trace listing subsequently expressed in those terms. Trace values can also be represented relative to a symbol. The same principles are extendable to handle memory segment offsets invoked by memory management units that automatically convert a relocated virtual address emitted by a processor into a dynamically adjusted run time physical address actually sent to the memory. According to a preferred embodiment of the invention the analyzer makes use of various symbol tables produced by any associated assemblers and compilers, as well as of any additional special symbol definitions desired by the user. The analyzer provides absolute values for these symbols by application of the load map produced during the relocation of the various programs into the target system monitored by the logic analyzer.

12 Claims, 6 Drawing Figures

