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(54) **CONTACT RESISTANCE REDUCTION TECHNIQUE**

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(58) **Field of Classification Search**

CPC H01L 29/7848; H01L 2029/7858; H01L 21/0245

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See application file for complete search history.

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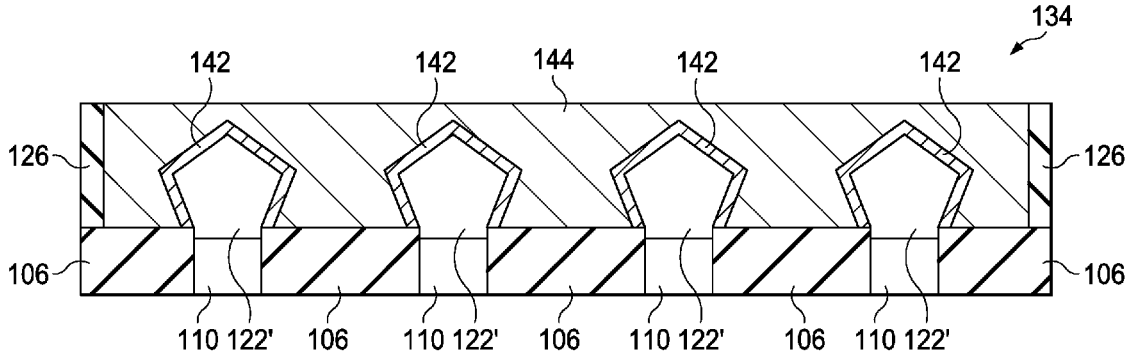
(57) **ABSTRACT**

An embodiment is a method of manufacturing a semiconductor device, the method including forming a first gate over a substrate, forming a recess in the substrate adjacent the first gate, epitaxially forming a strained material stack in the recess, the strained material stack comprising at least three layers, each of the at least three layers comprising a dopant. The method further includes co-implanting the strained material stack with dopants comprising boron, germanium, indium, tin, or a combination thereof, forming a metal layer on the strained material stack, and annealing the metal layer and the strained material stack forming a metal-silicide layer.

20 Claims, 14 Drawing Sheets