SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD FOR SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device that has both a bipolar transistor and a complementary-type field-effect transistor (hereinafter referred to as a CMOS transistor) formed on a semiconductor substrate, and to a method of manufacturing such as semiconductor device.

2. Background of the Invention

A technology in which the high operating speed and high drive capability of a bipolar transistor are combined with the low power consumption of a CMOS transistor, these being formed on one and the same substrate, is a known technology, referred to hereinafter as BiCMOS, and in recent years this has come to be a most effective means of meeting demands for low power consumption and high speed.

The prior art in this field will be described in terms of the structure of and manufacturing method for BiCMOS devices of recent years, reference being made to drawings FIG. **10** through FIG. **12**. This technology, described below, will be referred to as the first prior art, the cross-sectional views in FIG. **10** through FIG. **12** illustrating the sequence of manufacturing process steps for such as BiCMOS device. The description that follows will also include the structure of a BiCMOS device.

As shown in FIG. **10**(*a*), an isolation oxide film **302**, and a first oxide film **303** are formed on the surface of a p-type silicon substrate **301**, using a known LOCOS isolation method, a trench isolation method, or the like. Next, using boron ion implantation and heat treating, a first p-type well region **304** is formed in an n-channel MOS (NMOS) transistor forming region, and by phosphorus ion implantation and heat treating, a first n-type well region **305** is formed in a p-channel MOS (PMOS) transistor forming region and bipolar transistor collection region.

Next, as shown in FIG. **10**(*b*), a gate oxide film **306** is formed on the surface of the silicon substrate **301**, and a first polysilicon **307** is grown. Then, as shown in FIG. **10**(*c*), using photoresist or the like, a gate electrode **308** is formed, using a known anisotropic etching method. Then, as shown in FIG. **10**(*d*), boron ion implantation is used to form a p-type intrinsic base region **309**, after which ion implantation is done with photoresist or the like as a mask, so as to form an n-type LDD layer **310** and p-type LDD layer **311**, and formed a second oxide film **312** on the surface of the silicon substrate **301**.

Next, as shown in FIG. **11**(*a*), using photoresist or the like as a mask, a known etching technology is used to selectively remove the gate oxide film **306** and the second oxide film **312**, forming an emitter contact **313** and a collector contact **314**, a second polysilicon **315** being deposited as either a non-doped layer or as a layer doped with a dopant such as phosphor or arsenic.

Next, as shown in FIG. **11**(*b*), using photoresist or the like as a mask, a known anisotropic etching method is used to form an emitter electrode **316**, after which, using the above-noted photoresist mask and the second oxide film **312** as a mask forming a collector trench, etching is performed under the same etching conditions or in a plurality of steps, so as to etch the first n-type well region **305**, and form the collector trench **317**.

Next, as shown in FIG. **11**(*c*), after depositing a third oxide film **318**, a known anisotropic dry etching, that is, etch back, is used to form on each of the side walls of the emitter electrode **316** and collector trench **317** a side wall insulation film that is formed by an oxide film **318**, and form a side wall insulation film **319** that is formed as a laminate of the second oxide film **312** and the third oxide film **318** on the side wall of the gate electrode **308**.

Next, as shown in FIG. **11**(*d*), masking is done with photoresist or the like and a thin intervening oxide film **320** for ion implantation of an dopant such as phosphorus or arsenic, thereby forming on the NMOS n+ type source/drain **321** and on the bottom of the collector trench **317** an n+ type diffusion layer **322**, after which photoresist or the like is used as a mask for ion implantation of a dopant such as boron or BF_2, thereby forming the PMOS p+type source/drain **323** and p+ type extrinsic base **324**.

In the case of forming the above-noted second polysilicon **315** that forms the emitter electrode **316** by using a non-doped deposition, the introduction of a dopant into the emitter electrode **316** can also be done when forming the NMOS n+ type source/drain **321** by using ion implantation of phosphorus, arsenic or the like, and can also be done in a separately added process step in which phosphorus, arsenic or the like is introduced.

Next, as shown in FIG. **12**(*a*), a known method is used with a metal such as titanium, cobalt, or nickel, to suicide the surfaces of the gate electrode **308**, the emitter electrode **316**, n+ type diffusion layer **322** on the bottom of the collector trench **317**, the n+ type source/drain **321** and p+ type source/drain **323** and the p+ type extrinsic base **324**, forming the silicide layer **325**.

Next, as shown in FIG. **12**(*b*), an interlayer insulation film **326** made of a BPSG (boron-phosphorus-silicate-glass) film is formed and RTA (rapid thermal annealing) to form an emitter diffusion layer **327**, after which a contact hole is made, and a contact plug **328** is formed on an intervening barrier metal (not shown in the drawing), after which the metal wires **329** are formed.

Next, the BICMOS structure and associated method of manufacture that is noted in the Digest of Technical Papers, pp. 35–36, which is a pre-print of the IEEE 1997 Symposium on VLSI Technology, will be described, with reference being made to FIG. **13** and FIG. **14**. This technology, to be described below, will be referred to as the second prior art. FIG. **13** and FIG. **14** are cross-sectional views that show the sequence of manufacturing process steps for this BiCMOS structure. This will be described in terms of the same type of manufacturing processes as noted for the first prior art. Because of this relationship, items that are the same as in the first prior art are assigned the same reference numerals.

In this case, the process steps up until that shown in FIG. **10**(*c*) for the first prior art are the same. As shown in FIG. **13**(*a*), a mask of photoresist or the like is used with a known anisotropic etching method to form a gate electrode **308**. Then, ion implantation of boron or BF_2 and heat treating is done to form a p-type intrinsic base region **309** onto the surface of the first n-type well region **305**. Next, using a mask of photoresist or the like, ion implantation is done to form an n-type LDD layer **310** on the surface of the first p-type well region **304**, and a p-type LDD layer **311** on the surface of the first n-type well region **305**. Ion implantation is then done of, for example, phosphorus, with an energy of 70 keV and a dose of 1×10^{15} to 3×10^{16} cm^{-2} thereby forming a collector extension region **330**.

Next, as shown in FIG. **13**(*b*), a second oxide film **312** having a thick film thickness is deposited over the entire surface. Then, as shown in FIG. **13**(*c*), a mask of photoresist