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(54) **ENHANCEMENT MODE III-N HEMTS**

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(58) **Field of Classification Search**
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See application file for complete search history.

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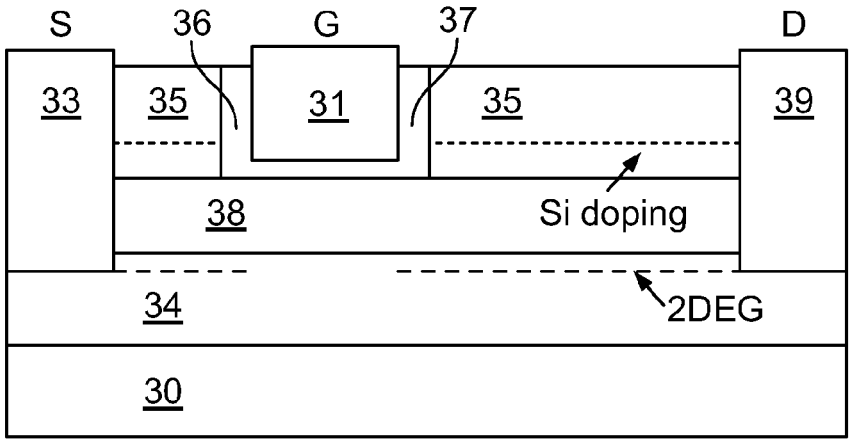
(57) **ABSTRACT**

A III-N semiconductor device that includes a substrate and a nitride channel layer including a region partly beneath a gate region, and two channel access regions on opposite sides of the part beneath the gate. The channel access regions may be in a different layer from the region beneath the gate. The device includes an AlXN layer adjacent the channel layer wherein X is gallium, indium or their combination, and a preferably n-doped GaN layer adjacent the AlXN layer in the areas adjacent to the channel access regions. The concentration of Al in the AlXN layer, the AlXN layer thickness and the n-doping concentration in the n-doped GaN layer are selected to induce a 2DEG charge in channel access regions without inducing any substantial 2DEG charge beneath the gate, so that the channel is not conductive in the absence of a switching voltage applied to the gate.

58 Claims, 15 Drawing Sheets