US009543437B2

(12) **United States Patent**
Choi et al.

(10) **Patent No.: US 9,543,437 B2**
(45) **Date of Patent: Jan. 10, 2017**

(54) **INTEGRATED CIRCUIT WITH DUAL STRESS LINER BOUNDARY**

(71) Applicant: **Texas Instruments Incorporated**, Dallas, TX (US)

(72) Inventors: **Youn Sung Choi**, Plano, TX (US); **Greg Charles Baldwin**, Plano, TX (US)

(73) Assignee: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/863,249**

(22) Filed: **Sep. 23, 2015**

(65) **Prior Publication Data**

US 2016/0013314 A1 Jan. 14, 2016

Related U.S. Application Data

(60) Continuation of application No. 14/478,144, filed on Sep. 5, 2014, now Pat. No. 9,171,901, which is a division of application No. 13/288,664, filed on Nov. 3, 2011, now Pat. No. 8,859,357.

(60) Provisional application No. 61/409,583, filed on Nov. 3, 2010.

(51) **Int. Cl.**

H01L 21/00	(2006.01)
H01L 29/78	(2006.01)
H01L 21/8238	(2006.01)
H01L 27/02	(2006.01)
H01L 27/092	(2006.01)
H01L 29/06	(2006.01)
H01L 29/10	(2006.01)

(52) **U.S. Cl.**
CPC ... ***H01L 29/7843*** (2013.01); ***H01L 21/823807*** (2013.01); ***H01L 27/0203*** (2013.01); ***H01L 27/092*** (2013.01); ***H01L 29/0638*** (2013.01); ***H01L 29/1033*** (2013.01)

(58) **Field of Classification Search**
CPC . H01L 29/7843; H01L 29/0638; H01L 27/092
See application file for complete search history.

(56) **References Cited**

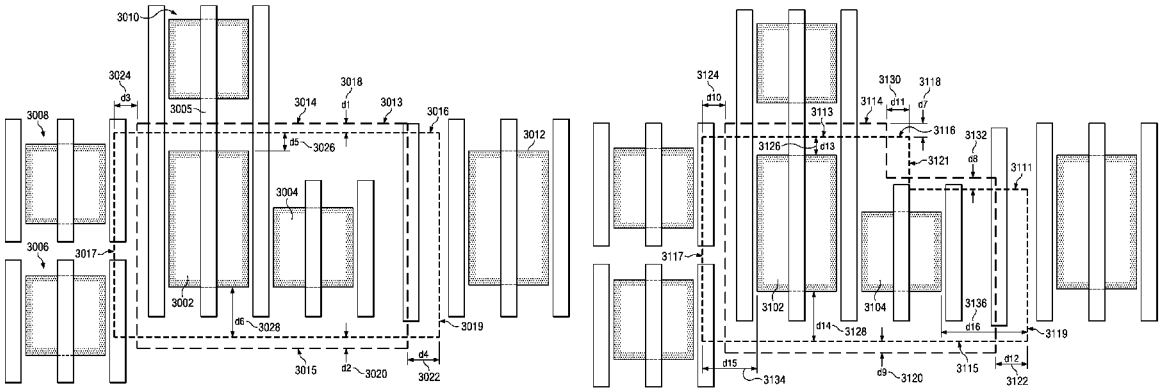
U.S. PATENT DOCUMENTS

7,355,262	B2 *	4/2008	Ko	H01L 21/324 257/374
7,514,752	B2 *	4/2009	Kohyama	H01L 21/823807 257/351
7,880,207	B2 *	2/2011	Fertig	H01L 27/1462 257/293
7,960,223	B2 *	6/2011	Chen	H01L 21/823807 257/E21.637
8,299,556	B2 *	10/2012	Fertig	H01L 25/043 136/255
8,735,241	B1 *	5/2014	Flachowsky	H01L 21/823807 438/199
8,859,357	B2 *	10/2014	Choi	H01L 21/823807 438/128

(Continued)

Primary Examiner — Laura Menz
(74) *Attorney, Agent, or Firm* — Tunelap Daniel Chan; Frank D. Cimino

(57) **ABSTRACT**

An integrated circuit with DSL borders perpendicular to the transistor gates primarily inside the nwell and with DSL borders parallel to the transistor gates primarily outside the nwell. A method for forming an integrated circuit with DSL borders perpendicular to the transistor gates primarily inside the nwell and with DSL borders parallel to the transistor gates primarily outside the nwell.

7 Claims, 5 Drawing Sheets