

What is claimed is:

1. A memory module comprising:

a plurality of memory devices, each memory device having a corresponding load; and

a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, the circuit selectively isolating one or more of the loads of the memory devices from the computer system, the circuit comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects.

2. The memory module of claim 1, wherein the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD).

3. The memory module of claim 2, wherein the circuit further comprises one or more switches operatively coupled to the logic element to receive control signals from the logic element.

4. The memory module of claim 1, wherein the plurality of memory devices has a first number of memory devices, and the circuit selectively isolates the loads of a second number of the memory devices from the computer system, the second number less than the first number.

5. The memory module of claim 4, wherein the first number of memory devices are configured in a plurality of ranks, and wherein the second number of memory devices are configured as one rank of the plurality of ranks.

6. The memory module of claim 1, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

7. The memory module of claim 1, wherein the plurality of memory devices are arranged in one or more ranks and the system memory domain is compatible to a first memory density per rank, and the physical memory domain is compatible with a second memory density per rank equal to twice the first memory density per rank.

8. The memory module of claim 1, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

9. The memory module of claim 1, wherein the memory module comprises a dual inline memory module.

10. The memory module of claim 9, wherein the memory module comprises a rank-buffered dual inline memory module.

11. The memory module of claim 1, wherein the memory module comprises a DDR2 SDRAM memory array.

12. The memory module of claim 1, wherein the circuit selectively isolates the loads of the memory devices from the computer system in response to a command or address signal received from the computer system.

13. A method of using a memory module with a computer system, the method comprising:

providing a memory module having a plurality of memory devices and a circuit electrically coupled to the plurality of memory devices, the circuit configured to be electrically coupled to a computer system, each memory device having a corresponding load;

electrically coupling the memory module to the computer system; and

activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects.

14. The method of claim 13, wherein the plurality of memory devices comprises a pair of memory devices, each memory device of the pair having a first memory capacity, the pair of memory devices configured to simulate a memory device having a second memory capacity equal to twice the first memory capacity.

15. The method of claim 13, wherein the logic translates address signals in the system memory domain to address signals in the physical memory domain.

16. The method of claim 13, wherein the plurality of memory devices are arranged in one or more ranks and the system memory domain is compatible to a first memory density per rank, and the physical memory domain is compatible with a second memory density per rank equal to twice the first memory density per rank.

17. The method of claim 13, wherein the memory module comprises a dual inline memory module.

18. A memory module connectable to a computer system, the memory module comprising:

a first memory device having a first data signal line and a first data strobe signal line;

a second memory device having a second data signal line and a second data strobe signal line;

a common data signal line connectable to the computer system; and

a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line, the device selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the device comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first, number of chip selects.

19. The memory module of claim 18, wherein the device comprises a logic element.

20. The memory module of claim 19, wherein the logic element is selected from the group consisting of: an application-specific integrated circuit, a custom-programmable logic device, and a field-programmable gate array.

21. The memory module of claim 18, wherein the device selectively electrically couples the first data signal line to the common data signal line and selectively electrically couples the second data signal line to the common data signal line.

22. The memory module of claim 18, wherein the memory module further comprises a common data strobe signal line connectable to the computer system, the device electrically coupled to the first data strobe signal line, to the second data strobe signal line, and to the common data strobe signal line, the device selectively electrically coupling the first data strobe signal line to the common data strobe signal line and selectively electrically coupling the second data strobe signal line to the common data strobe signal line.