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Matsumoto

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[54] PROCESS FOR FABRICATING BI-CMOS INTEGRATED CIRCUIT

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[52] U.S. Cl. 437/59; 257/552

[58] Field of Search 437/59; 357/43

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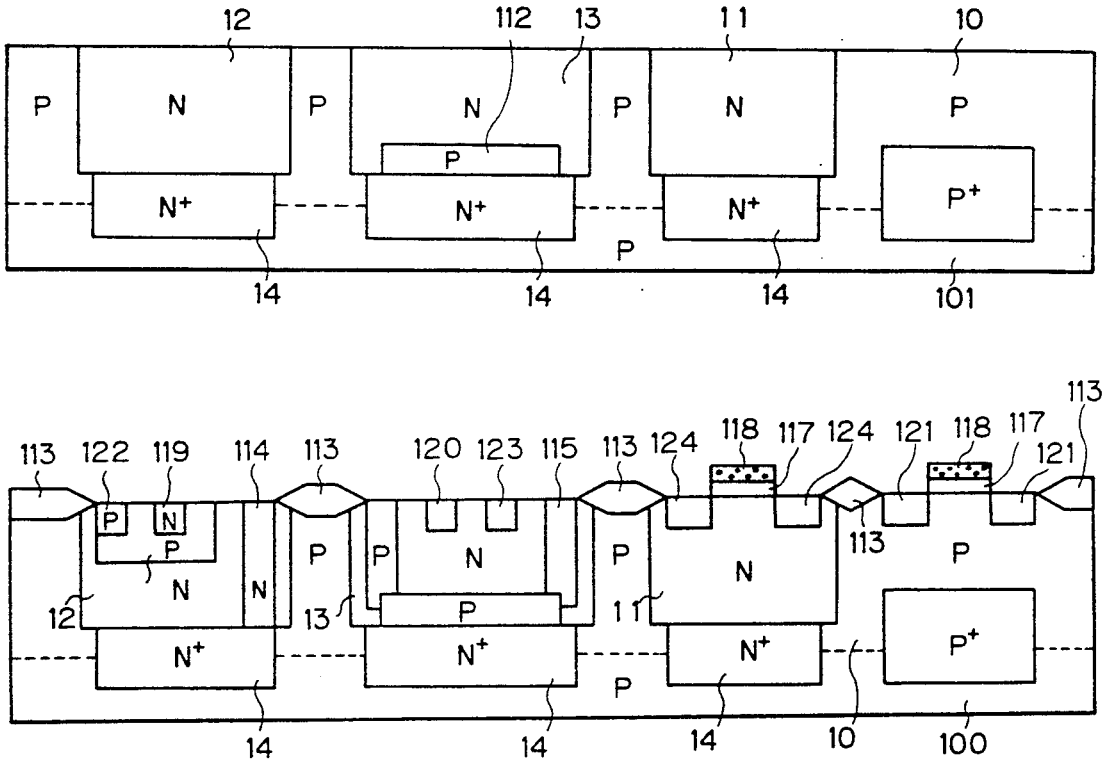
[57] ABSTRACT

A process for fabricating a Bi-CMOS integrated circuit according to the present invention comprises the steps of growing a P-type epitaxial layer after formation of buried layers, forming N-type diffusion layers in the epitaxial layer for forming the P-channel MOS transistor, an NPN transistor and a PNP transistor.

8 Claims, 10 Drawing Sheets