GATE METAL ROUTING FOR TRANSISTOR WITH CHECKERBOARDED LAYOUT

TECHNICAL FIELD

The present disclosure relates to semiconductor device structures and processes for fabricating high-voltage transistors.

BACKGROUND

High-voltage, field-effect transistors (HVFETs) are well known in the semiconductor arts. Many HVFETs employ a device structure that includes an extended drain region that supports or blocks the applied high-voltage (e.g., several hundred volts) when the device is in the "off" state. In a conventional vertical HVFET structure, a mesa or pillar of semiconductor material forms the extended drain or drift region for current flow in the on-state. A trench gate structure is formed near the top of the substrate, adjacent the sidewall regions of the mesa where a body region is disposed above the extended drain region. Application of an appropriate voltage potential to the gate causes a conductive channel to be formed along the vertical sidewall portion of the body region such that current may flow vertically through the semiconductor material, i.e., from a top surface of the substrate where the source region is disposed, down to the bottom of the substrate where the drain region is located.

In a traditional layout, a vertical HVFET consists of long continuous silicon pillar structure that extends across the semiconductor die, with the pillar structure being repeated in a direction perpendicular to the pillar length. One problem that arises with this layout, however, is that it tends to produce large warping of the silicon wafer during high temperature processing steps. In many processes, the warping is permanent and large enough to prevent the wafer from tool handling during subsequent processing steps.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure will be understood more fully from the detailed description that follows and from the accompanying drawings, which however, should not be taken to limit the invention to the specific embodiments shown, but are for explanation and understanding only.

FIG. **1** illustrates an example cross-sectional side view of a vertical HVFET structure.

FIG. **2**A illustrates an example layout of the vertical HVFET structure shown in FIG. **1**.

FIG. **2**B is an expanded view of one portion of the example layout shown in FIG. **2**A.

FIG. **3**A illustrates another example layout of the vertical HVFET structure shown in FIG. **1**.

FIG. **3**B is an expanded view of one portion of the example layout shown in FIG. **3**A.

FIG. **4**A illustrates yet another example layout of the vertical HVFET structure shown in FIG. **1**.

FIG. **4**B is an expanded view of one portion of the example layout shown in FIG. **4**A.

FIG. **5** illustrates an example layout of a wafer with die-to-die checkerboarding of HVFETs.

FIG. **6** illustrates an example layout of a wafer with die-to-die checkerboarding of segmented HVFETs.

FIG. **7** illustrates an example layout of a rectangular die with checkerboarded blocks of HVFET segments.

FIG. **8** illustrates an example gate metal routing layout for the die shown in FIG. **7**.

FIG. **9** illustrates an example gate and source metal routing layout for the die shown in FIG. **7**.

FIG. **10** illustrates an expanded portion of the example layout shown in FIG. **9**.

DETAILED DESCRIPTION

In the following description specific details are set forth, such as material types, dimensions, structural features, processing steps, etc., in order to provide a thorough understanding of the present invention. However, persons having ordinary skill in the relevant arts will appreciate that these specific details may not be needed to practice the present invention. It should also be understood that the elements in the figures are representational, and are not drawn to scale in the interest of clarity.

FIG. **1** illustrates an example cross-sectional side view of a vertical HVFET **10** having a structure that includes an extended drain region **12** of N-type silicon formed on an N+ doped silicon substrate **11**. Substrate **11** is heavily doped to minimize its resistance to current flowing through to the drain electrode, which is located on the bottom of the substrate in the completed device. In one embodiment, extended drain region **12** is part of an epitaxial layer that extends from substrate **11** to a top surface of the silicon wafer. A P-type body region **13** and N+ doped source regions **14***a* & **14***b* laterally separated by a P-type region **16**, are formed near a top surface of the epitaxial layer. As can be seen, P-type body region **13** is disposed above and vertically separates extended drain region **12** from N+ source regions **14***a* & **14***b* and P-type region **16**.

In one embodiment, the doping concentration of the portion of epitaxial layer which comprises extended drain region **12** is linearly graded to produce an extended drain region that exhibits a substantially uniform electric-field distribution. Linear grading may stop at some point below the top surface of the epitaxial layer **12**.

Extended drain region **12**, body region **13**, source regions **14***a* & **14***b* and P-type region **16** collectively comprise a mesa or pillar **17** (both terms are used synonymously in the present application) of silicon material in the example vertical transistor of FIG. **1**. Vertical trenches formed on opposite sides of pillar **17** are filled with a layer of dielectric material (e.g., oxide) that makes up dielectric region **15**. The height and width of pillar **17**, as well as the spacing between adjacent vertical trenches may be determined by the breakdown voltage requirements of the device. In various embodiments, mesa **17** has a vertical height (thickness) in a range of about 30 μm to 120 μm thick. For example, a HVFET formed on a die approximately 1 mm×1 mm in size may have a pillar **17** with a vertical thickness of about 60 μm. By way of further example, a transistor structure formed on a die of about 2 mm-4 mm on each side may have a pillar structure of approximately 30 μm thick. In certain embodiments, the lateral width of pillar **17** is as narrow as can be reliably manufactured (e.g., about 0.4 μm to 0.8 μm wide) in order to achieve a very high breakdown voltage (e.g., 600-800V).

In another embodiment, instead of arranging P-type region **16** between N+ source regions **14***a* & **14***b* across the lateral width of pillar **17** (as shown in FIG. **1**), N+ source regions and P-type regions may be alternately formed at the top of pillar **17** across the lateral length of pillar **17**. In other words, a given cross-sectional view such as that shown in FIG. **1** would have either an N+ source region **14**, or a P-type region **16**, that extends across the full lateral width of pillar **17**, depending upon where the cross-section is taken. In such an embodiment, each N+ source region **14** is adjoined on both sides