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(54) **METHOD AND STRUCTURE OF MAKING ENHANCED UTBB FDSOI DEVICES**

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(58) **Field of Classification Search**

CPC H01L 29/1033; H01L 29/0649; H01L 29/0653; H01L 29/0847; H01L 29/66575; H01L 29/7838

See application file for complete search history.

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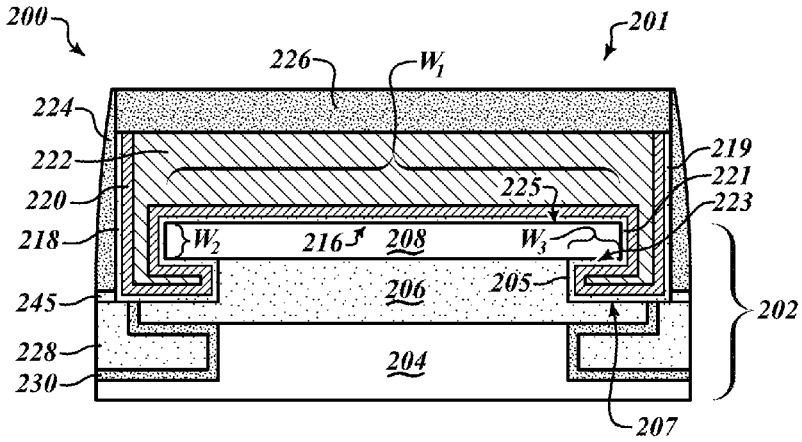
(57) **ABSTRACT**

An integrated circuit die includes a substrate having a first layer of semiconductor material, a layer of dielectric material on the first layer of semiconductor material, and a second layer of semiconductor material on the layer of dielectric material. An extended channel region of a transistor is positioned in the second layer of semiconductor material, interacting with a top surface, side surfaces, and potentially portions of a bottom surface of the second layer of semiconductor material. A gate dielectric is positioned on a top surface and on the exposed side surface of the second layer of semiconductor material. A gate electrode is positioned on the top surface and the exposed side surface of the second layer of semiconductor material.

21 Claims, 20 Drawing Sheets