In one implementation of the structure shown in FIG. **7**, each of the drift regions **82** has a width in the range of 0.4 μm to 3 μm, with a field plate width in a range of 1 μm to 3 μm, and a dielectric width (on either side of field plate **84**) in a range of 2 μm to 5 μm. These same dimensions may apply to the other embodiments discussed below. Thus, an HVFET fabricated in accordance with the present invention may have an edge termination area—defined as the distance between the edge of an outermost drift region to the scribe area of the die—of about 13 μm or less.

Another embodiment of an edge termination structure that mitigates electric field crowding in accordance with the present invention is shown in the cross-sectional perspective view of FIG. **8**, in which pairs of the narrow mesa drift regions **82** are joined or connected at the ends. By way of example, FIG. **8** shows elongated drift regions **82***a* & **82***b* connected at the lateral end by a region **95**. Drift regions **82***c* & **82***d* (not shown) are similarly connected together at the lateral edge of the transistor. In this embodiment, field plate member **84***b* terminates abruptly in a fingertip area **99** at the edge of the HVFET, while field plate members **84***a* & **84***c* are connected at the edge of the HVFET by a field plate region **98**. The connected field plate members **84***a* & **84***c* also connect with every second, i.e., alternate, field plate member in the HVFET. Each alternate field plate member that is not connected together (e.g., members **84***b*, **84***d*, etc.) terminates abruptly in a fingertip area **99** at the edge of the HVFET. As before, dielectric layer **88** surrounds both sides of the field plate members and includes curved corner areas and indented portions (e.g., **93***c*) that follow the shape of the connecting field plate region **98**. In this way, every cross-section of the edge termination structure shown in FIG. **8**, taken through the shortest line from one field plate member through a drift region to the next field plate member, is substantially the same.

FIG. **9** is a cross-sectional perspective view of a vertical HVFET device with an edge termination structure according to another embodiment of the present invention. The edge termination structure of FIG. **9** is similar to that shown in FIG. **8**, except that instead of connecting pairs of drift regions **82** together at the lateral ends, the embodiment of FIG. **9** connects all of the drift regions **82** together with a lateral connecting region **122**. All of the interior field plate members, i.e., **84***b*, **84***c*, etc., terminate abruptly in a fingertip area **99** at the lateral edge of the HVFET. The outer two field plate members (i.e., **84***a* and the other outer field plate member not shown) are connected together at the edge of the HVFET by a field plate region **104**. Thus, in the embodiment of FIG. **8**, the outermost field plate members are connected to form a contiguous ring that completely encircles the interior drift regions **82** and interior field plate members. (The words "ring" and "encircle" in this context do not necessarily mean that the field plate is circular or oval in shape or pattern. In the context of the present application, the words "ring" and "encircle" are intended to denote any laterally surrounding shape or pattern, be it circular, oval, rectilinear, etc.)

FIG. **10** is a top view of a vertical HVFET device with an edge termination structure according to yet another embodiment of the present invention. In this embodiment, each of the drift regions **82**, dielectric regions **88**, and field plate members **84** are formed as contiguous regions that are arranged in a concentric manner. For example, contiguous dielectric region **88***a* concentrically encircles interior drain substrate region **81***a*, contiguous field plate member **84***a* concentrically encircles dielectric region **88***a*, contiguous dielectric region **88***b* concentrically encircles field plate member **84***a*, contiguous drift region **82** concentrically encircles dielectric region **88***b*, contiguous dielectric region **88***c* concentrically encircles drift region **82**, contiguous field plate member **84***b* concentrically encircles dielectric region **88***c*, contiguous dielectric region **88***d* concentrically encircles dielectric region **88***b*, and exterior drain substrate region **81***b* concentrically encircles dielectric region **88***b*.

It is appreciated that the concentric regions described above may begin with an interior drain substrate region **81***a*, i.e., at the center of the HVFET, that is circular or oval in shape. The minimum radius of curvature at the edges or corner areas may be set to avoid high electric fields. Regardless of the shape of the innermost substrate region **81***a*, the contiguous regions may progressively become more square or rectangular in shape moving toward the outermost substrate region **81***b*. Furthermore, although the embodiment of FIG. **10** illustrates a single drift region **82**, the device structure is not limited in this regard; rather, there may be multiple, contiguous drift regions, each one progressively larger than the previous one moving toward the outer edge of the HVFET.

Although the present invention has been described in conjunction with specific embodiments, those of ordinary skill in the semiconductor device and fabrication arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

I claim:

1. A high-voltage transistor comprising:

a substrate having a top surface;

a drain of a first conductivity type;

a plurality of source regions of the first conductivity type;

a plurality of drift regions of the first conductivity type, each extending in a vertical direction from the drain toward the source, adjacent ones of the drift regions being separated in a first lateral direction by a dielectric layer, each of the drift regions terminating in a second lateral direction in a fingertip area;

a plurality of body regions of a second conductivity type, each body region separating a corresponding one of the source regions from a corresponding one of the drift regions;

a field plate member disposed within the dielectric layer that surrounds each of the drift regions in the first and second lateral directions, the field plate member having an entire length that extends in the vertical direction from a beginning at the top surface of the substrate downward to a farthest end of the field plate member, an inner region of the dielectric layer laterally separating the drift regions from the field plate member and an outer region of the dielectric layer laterally separating the field plate member from a perimeter semiconductor region of the substrate that extends in the vertical direction downward from the top surface, the perimeter semiconductor region being of the first conductivity type, the inner and outer regions each having a width that is substantially the same at all points along the entire length of the field plate member; and

a plurality of gates, each gate being disposed in the dielectric layer adjacent to and insulated from a corresponding one of the body regions, application of a voltage potential to the gate causing a vertical conduction channel to form in the body region such that current flows between the source regions and the drain when the high-voltage transistor is in an on-state.

2. The high-voltage transistor according to claim **1** wherein the fingertip area has a rounded shape.