

SERIAL INPUT OUTPUT (SIO) PORT EXPANSION APPARATUS AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to Serial input/output (SIO) data stream devices and methods. More particularly, the invention relates to devices and methods that allow SIO data streams to be delivered by a single SIO initiator device to multiple SIO target devices.

2. Description of the Related Art

Serial input/output (SIO) refers to a method of communicating data between devices in which the individual data bits are sent sequentially from an initiator device to a target device. Serial General Purpose Input Output (SGPIO) refers to serializing general purpose IO signals, e.g., by defining the communication between the initiator device, such as a host bus adapter (HBA), and the target device, such as a hard drive slot backplane or other backplane holding hard disk drives (HDDs). The data bus as specified by SGPIO typically is a four-signal (or four-wire) bus between the host bus adapter and the backplane. Of the four signals, three are driven by the host bus adapter and one is driven by the backplane. Typically, the host bus adapter is a storage controller located inside a server, desktop, rack or workstation computer. The host bus adapter interfaces with the hard disk drives to store and retrieve data.

The SGPIO specification is maintained by the SFF (Small Form Factor) Committee, and its official name of the SGPIO specification is SFF-8485. Within the SGPIO specification, the International Blinking Pattern Interpretation (IBPI) defines how SGPIO data streams are interpreted into states and how light emitting diodes (LEDs) on a backplane interpret these states as status indicators.

In conventional SIO communication system arrangements, a single initiator device typically is coupled to a single target device via an SGPIO bus or other appropriate bus coupled therebetween. Therefore, as the number of target devices within an SIO system increases, the number of initiator devices must increase accordingly. Such an increase in the number of initiator devices increases overall system complexity and costs, while also reducing overall system efficiency.

In data transmission environments that do not use SIO data streams, a port expander storage device, such as a Serial Attached SCSI (SAS) expander, can be used to couple a single initiator device to a plurality of target devices. SCSI refers to the Small Computer Systems Interface set of electronic interface standards that allow various devices to communicate with one another, e.g., computers to communicate with peripheral devices. However, like conventional SIO communication system arrangements, data transmission between a SAS initiator device and a plurality of SAS target devices still is based on a one-to-one relationship between the initiator device and the target devices. That is, the SAS expander receives and stores a data transmission from the SAS initiator device and then routes or directs the stored data to only one of the plurality of SAS target devices at any given time. Thus, although the SAS expander allows a SAS initiator device to be coupled to and communicate with a plurality of SAS target devices, the data transmitted from the SAS initiator device and stored in the SAS expander can be delivered only to one SAS target device at any given time.

SUMMARY OF THE INVENTION

The invention is embodied in an expander device and method for transmitting serial input/output (SIO) data

between an initiator device and a plurality of target devices. The expander device includes a processor/controller that is configured to receive a master data stream from an initiator device and to transmit a returning master data stream to the initiator device. The expander device also includes a plurality of target master ports that are coupled to the processor/controller and each configured to transmit a split data stream to a target device coupled thereto and to receive a returning split data stream from the target device coupled thereto. The processor/controller is configured to split the master data stream into a plurality of split data streams and to transmit the split data streams to the plurality of target master ports based on the split data streams. The processor/controller also is configured to assemble a plurality of returning split data streams into the returning master data stream and to transmit the returning master data stream to the initiator device. More specifically, the processor/controller splits the master data stream into a first split data stream having a first set of data bits, a second split data stream having a second set of data bits, a third split data stream having a third set of data bits and an nth split data stream having an nth set of data bits. The processor/controller transmits the first split data stream to a first target master port, the second split data stream to a second target master port, the third split data stream to a third target master port and the nth split data stream to an nth target master port. The processor/controller also receives a first returning split data stream from the first target master port, a second returning split data stream from the second target master port, a third returning split data stream from the third target master port and an nth returning split data stream from the nth target master port. The processor/controller also assembles the returning master stream from the returning split data streams in such a way that the data bits from the first returning split data stream are located in a first bit position in the returning master stream, the data bits from the second returning split data stream are located in a second bit position in the returning master stream, the data bits from the third returning split data stream are located in a third bit position in the returning master stream and the data bits from the nth returning split data stream are located in an nth bit position in the returning master stream.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a conventional SGPIO bus arrangement between an initiator device and a target device;

FIG. 2 is a schematic view of a conventional SGPIO bus arrangement between a plurality of initiator devices and a corresponding plurality of target devices;

FIG. 3 is a schematic view of an SGPIO data bit stream;

FIG. 4 is a schematic view of an SGPIO bus arrangement between an initiator device and a plurality of target devices, according to embodiments of the invention;

FIG. 5 is a schematic view of an apparatus for transmitting SGPIO data between an initiator device and a plurality of target devices, according to embodiments of the invention;

FIG. 6 is a schematic view of various split data bit streams, according to embodiments of the invention; and

FIG. 7 is a block diagram of a method for transmitting SGPIO data between an initiator device and a plurality of target devices, according to embodiments of the invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

In the following description, like reference numerals indicate like components to enhance the understanding of the