

The method **100** also includes a step **106** of directing the plurality of split data streams to the appropriate target master ports **96** of the corresponding plurality of target master ports **96**. More specifically, the state machine **84** and/or other appropriate portions of the processor/controller **82** direct the first split data stream (resulting from the splitting step **104**) to the coupling device **96** coupled to the first target master port **96**, the second split data stream to the coupling device **96** coupled to the second target master port **96**, the third split data stream to the coupling device **96** coupled to the third target master port **96**, and the nth split data stream to the coupling device **96** coupled to the nth target master port **96**.

The method **100** also includes a step **108** of transmitting or delivering the plurality of split data streams to their respective target devices. Each of the plurality of master data ports **96** delivers the split data stream received thereby to the respective master data port **96** coupled thereto. For example, the first master data port **96** receives and delivers the first split data stream to the first target device, which is coupled to the first master data port **96**, e.g., via an appropriate SGPIO bus coupled therebetween. Similarly, the second master data port **96** receives and delivers the second split data stream to the second target device, e.g., via an appropriate SGPIO bus coupled therebetween. Also, the third master data port **96** receives and delivers the third split data stream to the third target device, e.g., via an appropriate SGPIO bus coupled therebetween, and the nth master data port **96** receives and delivers the nth split data stream to the nth target device, e.g., via an appropriate SGPIO bus coupled therebetween.

The method **100** also includes a step **110** of receiving a plurality of returning split data streams from the plurality of target devices. Each master data port **96** has an SGPIO input (SIO\_DATA\_IN) to receive a split data stream from the respective target device coupled to the master data port **96**, e.g., via an appropriate SGPIO bus.

The method **100** also includes a step **112** of assembling the returning split data streams into a returning or outgoing master data stream. The state machine **84** and/or other appropriate portions of the processor/controller **82** assemble at least a portion of the returning split data streams received by the target master ports **96** from their respective coupled targets into a return or outgoing master data stream for deliver back to the initiator device. The multiplexer (MUX) or other suitable coupling device **99** coupled between the target master ports **96** and the processor/controller **82** couples together the returning split data streams received by the target master ports **96** from the target devices to the processor/controller **82**.

According to embodiments of the invention, the processor/controller **82** assembles the returning split data streams into a returning or outgoing master data stream based on the sets of data bits in the returning split data streams. As discussed hereinabove, the processor/controller **82** assembles the data bits from the first returning split data stream delivered to the first target master port **96** as the first set of data bits in the returning master data stream. In a similar manner, the processor/controller **82** assembles the data bits from the second returning split data stream delivered to the second target master port **96** as the second set of data bits in the returning master data stream. Also, the processor/controller **82** assembles the data bits from the third returning split data stream delivered to the third target master port **96** as the third set of data bits in the returning master data stream, and assembles the data bits from the nth returning split data stream delivered to the nth target master port **96** as the nth set of data bits in the returning master data stream.

The method **100** also includes a step **114** of transmitting or delivering the assembled returning master data stream to the

initiator device. Once the processor/controller **82** has assembled the returning or outgoing master data stream from the returning split data streams, the state machine **84** and/or other appropriate portions of the processor/controller **82** transmits or delivers the returning or outgoing master data stream to the initiator device via the SIO\_DATA\_OUT output, e.g., over an SGPIO bus coupled between the expander device **80** and the initiator device.

Certain steps in the processes or process flows described in this specification naturally precede others for the invention to function as described. However, the invention is not limited to the order of the steps described if such order or sequence does not alter the functionality of the invention. That is, it is recognized that some steps may be performed before, after, or parallel (substantially simultaneously with) other steps without departing from the scope and spirit of the invention. In some instances, certain steps may be omitted or not performed without departing from the invention. Further, words such as “thereafter,” “then,” “next,” and other similar words are not intended to limit the order of the steps. These words simply are used to guide the reader through the description of the exemplary method. Also, one of ordinary skill in programming will be able to write computer code or identify appropriate hardware and/or circuits to implement the disclosed invention without difficulty, based on the flow charts and associated description in this specification. Therefore, disclosure of a particular set of program code instructions or detailed hardware devices is not considered necessary for an adequate understanding of how to make and use the invention. The inventive functionality of the claimed computer implemented processes is explained in more detail in the above description and in conjunction with the Figures, which may illustrate various process flows.

In one or more aspects, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted as one or more instructions or code on a non-transitory computer-readable medium. Non-transitory computer-readable media includes both computer storage media and communication media including any tangible medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other tangible medium that may be used to carry or store desired program code in the form of instructions or data structures and that may be accessed by a computer.

It will be apparent to those skilled in the art that many changes and substitutions can be made to the embodiments of the invention herein described without departing from the spirit and scope of the invention as defined by the appended claims and their full scope of equivalents.

The invention claimed is:

1. A serial input/output (SIO) expander device, comprising:
  - a processor/controller configured to receive a master data stream from an initiator device and to transmit a returning master data stream to the initiator device; and
  - a plurality of target master ports coupled to the processor/controller and configured to transmit a split data stream to a target device coupled thereto and to receive a returning split data stream from the target device coupled thereto,