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(54) **SERIAL INPUT OUTPUT (SIO) PORT EXPANSION APPARATUS AND METHOD**

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(52) **U.S. Cl.**
USPC **710/110**; 710/71; 710/74; 710/300

(58) **Field of Classification Search**
USPC 710/71, 74, 110, 300
See application file for complete search history.

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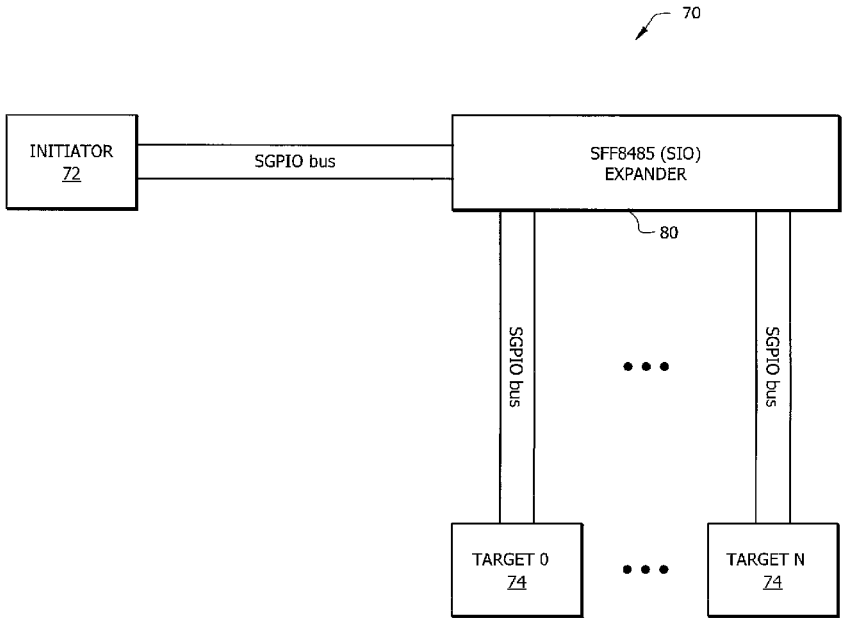
(57) **ABSTRACT**

An expander device and method for transmitting serial input/output (SIO) data between an initiator device and a plurality of target devices. The expander device includes a processor/controller configured to receive a master data stream from an initiator device and to transmit a returning master data stream to the initiator device. The expander device includes a plurality of target master ports coupled to the processor/controller and configured to transmit split data streams to corresponding target devices coupled thereto and to receive returning split data streams from the target devices. The processor/controller splits the master data stream, based on its data, into a plurality of split data streams, and directs the split data streams to the target master ports based on the data in the split data streams. The processor/controller also assembles a plurality of returning split data streams into the returning master data stream and transmits the returning master data stream to the initiator device.

20 Claims, 6 Drawing Sheets