METHOD AND APPARATUS FOR PREDICTING DEVICE ELECTRICAL PARAMETERS DURING FABRICATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the field of semiconductor device manufacturing and, more particularly, to a method and apparatus for predicting device electrical parameters during fabrication.

2. Description of the Related Art

There is a constant drive within the semiconductor industry to increase the quality, reliability and throughput of integrated circuit devices, e.g., microprocessors, memory devices, and the like. This drive is fueled by consumer demands for higher quality computers and electronic devices that operate more reliably. These demands have resulted in a continual improvement in the manufacture of semiconductor devices, e.g., transistors, as well as in the manufacture of integrated circuit devices incorporating such transistors. Additionally, reducing the defects in the manufacture of the components of a typical transistor also lowers the overall cost per transistor as well as the cost of integrated circuit devices incorporating such transistors.

Generally, a set of processing steps is performed on a wafer using a variety of processing tools, including photolithography steppers, etch tools, deposition tools, polishing tools, rapid thermal processing tools, implantation tools, etc. One technique for improving the operation of a semiconductor processing line includes using a factory wide control system to automatically control the operation of the various processing tools. The manufacturing tools communicate with a manufacturing framework or a network of processing modules. Each manufacturing tool is generally connected to an equipment interface. The equipment interface is connected to a machine interface which facilitates communications between the manufacturing tool and the manufacturing framework. The machine interface can generally be part of an advanced process control (APC) system. The APC system initiates a control script based upon a manufacturing model, which can be a software program that automatically retrieves the data needed to execute a manufacturing process. Often, semiconductor devices are staged through multiple manufacturing tools for multiple processes, generating data relating to the quality of the processed semiconductor devices. Pre-processing and/or post-processing metrology data is supplied to process controllers for the tools. Operating recipe parameters are calculated by the process controllers based on the performance model and the metrology information to attempt to achieve post-processing results as close to a target value as possible. Reducing variation in this manner leads to increased throughput, reduced cost, higher device performance, etc., all of which equate to increased profitability.

In a typical semiconductor fabrication facility, wafers are processed in groups, referred to as lots. The wafers in a particular lot generally experience the same processing environment. In some tools, all of the wafers in a lot are processed simultaneously, while in other tools the wafers are processed individually, but under similar conditions (e.g., using the same operating recipe). Typically, a lot of wafers is assigned a priority in the beginning of its processing cycle. Priority may be assigned on the basis of the number of wafers in the lot or its status as a test or experimental lot, for example.

At a particular processing step, the relative assigned priorities of all the lots ready for processing are compared. Various rules are applied to determine which of the eligible

lots is selected for processing. For example, for two lots with the same priority, the older of the lots is often selected for subsequent processing. In the case of a test lot of wafers (i.e., generally including a reduced number of wafers), the lot is subjected to one or more experimental processing steps or recipe adjustments in an attempt to improve the performance of the process or the performance of the resultant devices. Before commencing production of regular production lots using the experimental parameters, it is useful to first test the effectiveness of the changes based on the resulting characteristics of the wafers in the test lot. Hence, a test lot would be assigned a relatively high priority over other production lots, such that its processing is completed more quickly. Regardless of the particular priority assignments made, the rules are essentially static and predetermined. The priority of a particular lot does not typically change during its processing cycle, unless its status changes from being a production lot to a test lot, for example.

During the fabrication process various events may take place that affect the performance of the devices being fabricated. That is, variations in the fabrication process steps result in device performance variations. Factors, such as feature critical dimensions, doping levels, contact resistance, particle contamination, etc., all may potentially affect the end performance of the device. Devices are typically ranked by a grade measurement, which effectively determines its market value. In general, the higher a device is graded, the more valuable the device.

Because of the large number of variables affecting a device's performance characteristics, it is difficult to predict the grade of the device prior to the performing of electrical tests on the devices. Wafer electrical test (WET) measurements are typically not performed on processed wafers until quite late in the fabrication process, sometimes not until weeks after the processing has been completed. When one or more of the processing steps produce resulting wafers that the WET measurements indicate are unacceptable, the resulting wafers may need to be scrapped. However, in the meantime, the misprocessing might have gone undetected and uncorrected for a significant time period, leading to many scrapped wafers, much wasted material, and decreased overall throughput.

The present invention is directed to overcoming, or at least reducing the effects of, one or more of the problems set forth above.

SUMMARY OF THE INVENTION

One aspect of the present invention is seen in a method that includes providing a set of initial characteristic values associated with the semiconductor device. A first fabrication process is performed on the semiconductor device. Fabrication data associated with the first fabrication process is collected. At least one of the initial characteristic values is replaced with the fabrication data collected for the first fabrication process to generate a first modified set of characteristic values. A first value for at least one electrical characteristic of the semiconductor device is predicted based on the modified set of characteristic values.

Another aspect of the present invention is seen in a system including a first process tool, a first data collection unit, and a prediction unit. The first process tool is configured to perform a first fabrication process on the semiconductor device. The first data collection unit is configured to collect fabrication data associated with the first fabrication process. The prediction unit is configured to provide a set of initial characteristic values associated with the semiconductor device, replace at