down, lower power CPU is left operational during the active sleep mode state. Here, the scaled down, lower power CPU should have sufficient processing power so that any, some or all of the embodiments **250**, **260**, **270** of FIG. **2***a* and/or the methodologies of FIGS. **4***a* through **7***b* are possible.

Again, the on chip cache **908** is used as the system memory for the active sleep mode state. An active sleep mode interface **928** to communicate with I/O components in active sleep mode and a normal active interface **912** (e.g. front side bus) to communicate with I/O components during normal active mode may be kept separate (as observed in FIG. **9**); or, alternatively may be merged to at least some degree. Separate control/data lines **927**, **928** for displaying information during the active sleep mode state may be associated with the low CPU portion **921**. Again the circuitry for implementing the low end and high end CPUs **921**, **901** may be integrated onto the same semiconductor chip **940**.

Thus, It is to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the Central Processing Unit (CPU) of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method, comprising:

(a) transitioning a computing system from a normal active mode to an active sleep mode, said transitioning comprising:

storing active sleep mode software instructions to be executed by a low end central processing unit into an on chip cache that cached normal active mode software instructions that were executed by a high end central processing unit during said normal active mode, said active sleep mode software instructions to be executed by said low end central processing unit during said active sleep mode, said computing system consuming less power during said active sleep mode than during said normal active mode;

placing a graphics controller into a low power state in which said graphics controller will not perform graphics processing tasks in said active sleep mode that it performed in said normal active mode; and

(b) during said active sleep mode:

executing at least a portion of said active sleep mode instructions in order to wirelessly receive information;

transferring said information from a wireless interface to said on chip cache;

executing at least a second portion of said active sleep mode instructions in order to compress said information before it is stored externally from said cache.

2. The method in claim **1** further comprising executing at least a third portion of said active sleep mode instructions in order to decompress said information after it has been said stored.

3. The method in claim **1** wherein said information is said stored in a non volatile storage device.

4. The method in claim **3** wherein said non volatile storage device is a magnetic hard disk drive.

5. The method in claim **3** wherein said non volatile storage device is a FLASH memory.

6. The method in claim **1** further comprising executing at least a fourth portion of said active sleep mode instructions in order to display said information on a display unit.

7. A method, comprising:

(a) transitioning a computing system from a normal active mode to an active sleep mode, said transitioning comprising:

storing active sleep mode software instructions to be executed by a low end central processing unit into an on chip cache that cached normal active mode software instructions that were executed by a high end central processing unit during said normal active mode, said active sleep mode software instructions to be executed by said low end central processing unit during said active sleep mode, said computing system consuming less power during said active sleep mode than during said normal active mode;

placing a graphics controller into a low power state in which said graphics controller will not perform graphics processing tasks in said active sleep mode that it performed in said normal active mode; and

(b) during said active sleep mode:

executing at least a portion of said active sleep mode instructions in order to wirelessly receive information;

transferring said information from a wireless interface to said on chip cache;

transferring said information from said on chip cache to a non volatile storage device.

8. The method in claim **7** further comprising executing at least a second portion of said active sleep mode instructions in order to decompress said information after it has been said received.

9. The method in claim **7** further comprising executing at least a second portion of said active sleep mode instructions in order to compress said information before it is stored to said non volatile storage device.

10. The method in claim **9** wherein said non volatile storage device is a magnetic hard disk drive.

11. The method in claim **9** wherein said non volatile storage device is a FLASH memory.

12. The method in claim **7** further comprising executing at least a third portion of said active sleep mode instructions in order to display information on a display unit.

13. The method in claim **7** wherein said non volatile storage device is a magnetic hard disk drive.

14. The method in claim **7** wherein said non volatile storage device is a FLASH memory.

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