VERTICAL CHARGE CONTROL SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of power MOSFET is a DMOS (double-diffused metal oxide semiconductor) transistor. A cross-sectional view of a portion of a cell array of one known variety of DMOS transistors is shown in FIG. **1**. As shown, an n-type epitaxial layer **102** overlies n-type substrate region **100** to which the drain contact is made. Polysilicon-filled trenches extend into the epitaxial layer **102** from the top surface. The polysilicon **106***a*, **106***b* in the trenches are insulated from the epitaxial layer by oxide layers **104***a*, **104***b*. Source regions **108***a*, **108***b* in p-type body regions **110***a*, **110***b* are adjacent the trenches at the top surface. A polysilicon gate **114** overlaps the source regions **108***a,b*, extends over a surface portion of the body regions **110***a,b*, and extends over a surface area of a region between the two trenches commonly referred to as the mesa drift region. Metal layer **116** electrically shorts source regions **108***a,b* to body regions **110***a,b* and polysilicon **106***a,b* in the trenches. The surface area of body regions **110***a,b* directly underneath gate **114** defines the transistor channel region. The area between body regions **110***a* and **110***b* under gate **114** is commonly referred to as the JFET region.

Upon applying a positive voltage to the gate and the drain, and grounding the source and the body regions, the channel region is inverted. A current thus starts to flow from the drain to the source through the drift region and the surface channel region.

A maximum forward blocking voltage, hereinafter referred to as "the breakdown voltage", is determined by the avalanche breakdown voltage of a reverse-biased body-drain junction. The DMOS structure in FIG. **1** has a high breakdown voltage due to the polysilicon-filled trenches. Polysilicon **106***a,b* cause the depletion layer formed as a result of the reverse-biased body-drain junction to be pushed deeper into the drift region. By increasing the depletion region depth without increasing the electric field, the breakdown voltage is increased without having to resort to reducing the doping concentration in the drift region which would otherwise increase the transistor on-resistance.

A drawback of the FIG. **1** structure is its high output capacitance Coss, making this structure less attractive for high frequency applications such as radio frequency (RF) devices for power amplifiers in the wireless communication base stations. The output capacitance Coss of the FIG. **1** structure is primarily made up of: (i) the capacitance across the oxide between the polysilicon in the trenches and the drift region (i.e., Cox), in series with (ii) the capacitance across the depletion region at the body-drift region junction. Cox is a fixed capacitance while the depletion capacitance is inversely proportional to the body-drain bias.

The breakdown voltage of power MOSFETs is dependent not only upon the cell structure but also on the manner in which the device is terminated at its outer edges. To achieve a high breakdown voltage for the device as a whole, the breakdown voltage at the outer edges must be at least as high as that for the cells. Thus, for any cell structure, a corresponding terminating structure is needed which exhibits a high breakdown voltage.

In most amplifier circuits a significant amount of heat energy is produced in the transistor. Only 50% efficiency is typical of the best class AB RF power amplifiers available. An important factor in designing power devices for high frequency applications is thus the thermal performance of the device. Because of the different device performance requirements, the cells in power MOSFETs are densely packed resulting in concentration of heat in active regions and poor heat transfer rates. The increase in temperature resulting from the poor heat transfer rate adversely effects the device performance.

Thus, a power MOSFET device with such improved characteristics as low output capacitance, high breakdown voltage, and improved thermal performance is desired.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, MOSFET cell structures and edge termination structures, and methods of manufacturing the same, are described which among other features and advantages exhibit a substantially reduced output capacitance, high breakdown voltage, and improved thermal performance.

In one embodiment, a MOSFET comprises at least two insulation-filled trench regions laterally spaced in a first semiconductor region to form a drift region therebetween, and at least one resistive element located along an outer periphery of each of the two insulation-filled trench regions. A ratio of a width of each of the insulation-filled trench regions to a width of the drift region is adjusted so that an output capacitance of the MOSFET is minimized.

In another embodiment, a MOSFET comprises a first semiconductor region having a first surface, a first trench region extending from the first surface into the first semiconductor region, and at least one floating discontinuous region along a sidewall of the first trench region.

In another embodiment, a MOSFET comprises a first semiconductor region having a first surface, a first trench region extending from the first surface into the first semiconductor region, and a first plurality of regions along a sidewall of the first trench region.

In another embodiment, a MOSFET comprises a first semiconductor region having a first surface, and first and second insulation-filled trench regions each extending from the first surface into the first semiconductor region. Each of the first and second insulation-filled trench regions has an outer layer of silicon of a conductivity type opposite that of the first semiconductor region. The first and second insulation-filled trench regions are spaced apart in the first semiconductor region to form a drift region therebetween such that the volume of each of the first and second trench regions is greater than one-quarter of the volume of the drift region.

In another embodiment, a MOSFET comprises a first semiconductor region over a substrate. The first semiconductor region has a first surface. The MOSFET further includes first and second insulation-filled trench regions each extending from the first surface to a predetermined depth within the first semiconductor region. Each of the first and second insulation-filled trench regions has an outer layer of doped silicon material which is discontinuous along a bottom surface of the insulation-filled trench region so that the insulation material along the bottom surface of the insulation-filled trench region is in direct contact with the first semiconductor region. The outer layer of silicon material is of a conductivity type opposite that of the first semiconductor region.

In another embodiment, a MOSFET comprises a first semiconductor region having a first surface, a first