

TABLE 6

	←	Set 1	→	←	Set 2	→
	a ₁	b ₁	c ₁	a ₂	b ₂	c ₂
P1						
P2						

P1 and P2 are calculated according to equations (9) and (10) above—the second set of values does not add any extra computational overhead.

The result vector also has bit positions for the values of the two different sets:

TABLE 7

	←	Set 1	→	←	Set 2	→
	a ₁	b ₁	c ₁	a ₂	b ₂	c ₂
V1						

V1 is calculated according to equation (11) above, from P1 and P2. A true value at any particular bit position of the result vector indicates that the value corresponding to that particular bit position is the median value of its set. Thus, two sets of values can be evaluated in parallel after filling the relationship table as shown in Table 6.

Even further parallelism can be achieved with processors that support SIMD operations. Such processors allow parallel operations on wide registers having multiple words or bytes that, together, can include sixty-four or more bit positions. With sixty-four-bit rows such as those formed by SIMD registers, tables such as those discussed above can have sixty-four columns—thereby containing twenty-one sets of values (assuming three values a, b, and c in each set). In a more realistic example where each set has five values, twelve sets can be evaluated in parallel, thereby taking advantage of the parallel processing capacities of modern multimedia processors. In many situations, it may be more efficient to use a single word or byte of an MMX wide register for each set of values, even though some of the bit positions in each byte may not be used.

In light of the discussion and rather simple example given above, involving only three values in a particular set, the following discussion illustrates how to implement the invention to find median pixel values for sets comprised of five pixels. FIG. 1 shows a possible arrangement of pixels in which it is desired to find the median pixel value from five possible pixels a, b, c, d, and e.

The first step is to list the different possible sets of relationships that would be satisfied if any particular value were the median. For example, value a could be the median in any one of six different ways:

(12) (a>b) AND (a>c) AND (a<d) AND (a<e) or

(13) (a>b)AND(a>d)AND(a<c)AND(a<e) or

(14) (a>b) AND (a>c) AND (a<c) AND (a<d) or

(15) (a>c) AND (a>d) AND (a<b) AND (a<e) or

(16) (a>c)AND(a>e)AND(a<b)AND(a<d) or

(17) (a>d)AND(a>e)AND(a<b)AND(a<c)

Table 8 below shows corresponding groups of ANDed conditions for each of values a, b, c, d, and e. Each group of conditions under a given column, if satisfied, indicates that the value corresponding to the column is the median.

TABLE 8

	a	b	c	d	e
5	a > b	b > a	c > a	d > a	e > a
	a > c	b > c	c > b	d > b	e > b
	a < d	b < d	c < d	d < c	e < c
	a < e	b < e	c < e	d < e	e < d
	a > d	b > d	c > d	d > c	e > c
	a > e	b > e	c > e	d > e	e > d
10	a < b	b < a	c < a	d < a	e < a
	a < c	b < c	c < b	d < b	e < b
	a > b	b > a	c > a	d > a	e > a
	a > d	b > d	c > d	d > c	e > c
	a < c	b < c	c < b	d < b	e < b
	a < e	b < e	c < e	d < e	e < d
15	a > c	b > c	c > b	d > b	e > b
	a > e	b > e	c > e	d > e	e > d
	a < b	b < a	c < a	d < a	e < a
	a < d	b < d	c < d	d < c	e < c
	a > b	b > a	c > a	d > a	e > a
	a > e	b > e	c > e	d > e	e > d
20	a < c	b < c	c < b	d < b	e < b
	a < d	b < d	c < d	d < c	e < c
	a > c	b > c	c > b	d > b	e > b
	a > d	b > d	c > d	d > c	e > c
	a < b	b < a	c < a	d < a	e < a
	a < e	b < e	c < e	d < e	e < d

Table 8, referred to herein as an assignment table, can be used to arrange a relationship table and to determine which bit registers should be ANDed to form the parallel condition registers. Note that in this case, the relationship table will have eight rows or bit registers. The bit registers will be referred to as R1 through R8. There will be six parallel condition registers, referred to as P1 through P6. Generally, the number of parallel condition registers will be given by the equation

$$(n-1)! / \left[\left(\frac{n-1}{2} \right)! \right]^2, \tag{18}$$

where n is the number of available values from which a median is sought

The assignment table of Table 8 is augmented by assigning each listed inequality to one of the eight available bit registers. Starting with a single column, such as column a, the eight different possible relationships involving a are assigned to different bit registers or rows, as shown in Table 9. The eight different relationships in each of the other columns are also assigned to registers. The assignments are made so that each cell of a single row indicates the same set of bit registers: each cell of the first row indicates R1, R2, R3, and R4; each cell of the second row contains R5, R6, R7, and R8. For this to be possible, the second row should contain inequalities that are the inverse of those in the first row.

TABLE 9

	a	b	c	d	e
60	a > b→R1	b > a→R1	c > a→R1	d > a→R1	e > a→R1
	a > c→R2	b > c→R2	c > b→R2	d > b→R2	e > b→R2
	a < d→R3	b < d→R3	c < d→R3	d < c→R3	e < c→R3
	a < e→R4	b < e→R4	c < e→R4	d < e→R4	e < d→R4
	a > d→R5	b > d→R5	c > d→R5	d > c→R5	e > c→R5
	a > e→R6	b > e→R6	c > e→R6	d > e→R6	e > d→R6
	a < b→R7	b < a→R7	c < a→R7	d < a→R7	e < a→R7
65	a < c→R8	b < c→R8	c < b→R8	d < b→R8	e < b→R8
	a > b	b > a	c > a	d > a	e > a