example, power switching or integrated logic, negative polarity gate supply is undesired. Transistors may then work in enhancement mode (E-mode).

26 Claims, 10 Drawing Sheets

(51) **Int. Cl.**
H01L 29/20 (2006.01)
H01L 29/10 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7786*** (2013.01); *H01L 29/1066* (2013.01); *H01L 29/2003* (2013.01)

(58) **Field of Classification Search**
USPC 257/192, 194, E29.246, E21.403, 257/E21.407; 438/172
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

8,519,438	B2 *	8/2013	Mishra et al.	257/192
2004/0164317	A1	8/2004	Nishihori et al.	
2006/0043396	A1 *	3/2006	Tsuda et al.	257/94
2006/0083280	A1 *	4/2006	Tauzin	H01L 21/76254 372/46.01
2008/0093626	A1 *	4/2008	Kuraguchi	257/190
2009/0072272	A1	3/2009	Suh et al.	
2009/0146182	A1	6/2009	Hikita et al.	
2009/0194790	A1	8/2009	Sato et al.	
2010/0025730	A1	2/2010	Heikman et al.	
2010/0084687	A1 *	4/2010	Chen et al.	257/194
2012/0223320	A1 *	9/2012	Dora	H01L 29/1608 257/76
2013/0292686	A1 *	11/2013	Kizilyalli et al.	257/76

FOREIGN PATENT DOCUMENTS

EP	1424734	A2	2/2004
EP	1610392	A1	12/2005
JP	2001177089	A	6/2001
JP	2004179318	A	6/2004
JP	2004193273	A	7/2004
JP	2006121091		5/2006
JP	2009503815	A	1/2009
JP	2009188397	A	8/2009
WO	WO2007018918	A2	2/2007
WO	2009132039		10/2009

OTHER PUBLICATIONS

International Search Report from the European Patent Office, PCT/EP2012/063318 (Nov. 5, 2012).
David C. Hays, Selective Etching of Compound Semiconductors, University of Florida Masters Thesis, 1999, 1-138.
Notification of Reasons for Refusal, Mailing Date Mar. 22, 2016, English Translation of Japanese Patent Office Action in Application No. 2014-520602.
The State Intellectual Property Office of the People's Republic of China (SIPO), Search Report Dated Feb. 14, 2016, Application No. 201280035805.9, Application Date: Jul. 6, 2012, Applicant: EPIGAN NV, (1 page).

* cited by examiner