METHOD OF MAKING TOPOGRAPHIC PATTERN DELINEATED POWER MOSFET WITH PROFILE TAILORED RECESSED SOURCE

This is a division of application Ser. No. 07/194,874, filed May 17, 1988, now U.S. Pat. No. 4,895,810, issued Jan. 23, 1990, which is a continuation-in-part of commonly-assigned U.S. patent application of T. G. Hollinger, Ser. No. 06/842,771, filed Mar. 21, 1986, entitled MASK SURROGATE SEMICONDUCTOR PROCESS EMPLOYING DOPANT-OPAQUE REGION, now U.S. Pat. No. 4,748,103, issued May 31, 1988.

BACKGROUND OF THE INVENTION

This invention relates to a method for producing power semiconductor devices, and more particularly, to such a power MOSFET fabrication process and structure which substantially eliminates the incidence of fatal defects in a power device as a consequence of defects in, and/or misalignment between, the layers used in the production of such devices.

In the prior art fabrication of transistor devices on silicon wafers, such as power-MOS field-effect transistors, there have been significant problems in (1) obtaining an acceptably high yield of relatively large-current-capability transistors without (2) driving the cost of production to extremely high and unacceptable levels. A major contributor to this problem has been that the best known prior art fabrication techniques for making power MOSFET devices typically employ five or more independent masking, diffusion and metallization steps, each offering a significant opportunity for the creation of a fatal error in a device. Generally speaking, the more steps, the greater the likelihood of fatal defects; or conversely, the lower the yield of devices that operate within specifications. In high-current/high voltage power devices, it is especially important to avoid designs and defects that can lead to current leakage, shorting, high on-resistance or a wide variation in performance characteristics among nominally similar devices.

One cause of these defects is misalignment occurring during successive masking steps. Defects can also occur in situations where one or more of the masks or layers may, individually, have localized defects. Also, fatal defects can occur if airborne contaminants collect on a mask or a wafer. This possibility is also aggravated by the plurality of masking steps now required.

Gate and source contacts have been conventionally separated using masking or multiple layer techniques. These steps require critical alignment and/or an intermetallic dielectric such as oxide, PSG, BPSG, BSG, or other material such as polyimide. This approach, though effective and traditional, is complex and lends itself to excessive yield loss and cumbersome processing techniques. Also, the device structures that result from these techniques have a tendency to increase certain undesirable parasitic effects.

These problems make it difficult economically, with any expectation of achieving an acceptably high yield, to manufacture relatively large, high-current-capability devices. Put another way, the larger the design of the device, the greater is the likelihood that it will contain a fatal defect. To date, an economically practical size limit has been about 0.25 inches on each side of a device. Accordingly, the tendency in the past has been to reduce the size of individual devices to increase the

chances of a larger number of smaller devices surviving defects. However, these smaller devices, while emerging with an acceptable yield percentage, are capable only of handling relatively low-level currents, and thus low-power applications. Accordingly, they must be linked electrically in collections in some fashion in order to be able to handle relatively high-power applications.

Past efforts to improve the yield of larger-surface-area devices have primarily directed attention to performing the manufacturing steps in the cleanest possible environment, creating masks under extremely expensive manufacturing conditions, and improving mask alignment by use of very sophisticated, precise alignment machines. These areas of attention are extremely expensive, and, as a practical matter, make their use economically unattractive vis-a-vis the final market price which, as a consequence, must be attached to a finished device.

Accordingly, a need remains for a device structure and fabrication process that can produce high voltage solid-state power switches with increased yields in larger size to handle high current but without undesirable parasitic effects.

SUMMARY OF THE INVENTION

A general object of the present invention, therefore, is to provide a novel manufacturing procedure which is capable of reducing substantially the percentage likelihood that a fatal defect will occur in a final semiconductor device, even though that device may occupy the entire usable area (i.e., as a single device) on a substrate, such as a silicon wafer.

A related object is to provide such a procedure which offers a simple and very low-cost process enabling the production of high-yield, defect-free semiconductor devices which are capable individually of handling strikingly larger currents than are now practical.

Another object is to provide a power MOSFET structure and process with effective yet simple gate-to-source contact isolation.

An additional object is to improve power MOSFET device characteristics.

The key to the simplicity, effectiveness and cost advantage of the invention is that, according to one manner of practicing it, only a single, independent mask is required in the production of the usual plural, functional regions in a semiconductor device. According to another way of practicing the invention, no mask at all is required. A dopant-opaque region or layer, such as polysilicon on gate oxide on the upper surface of the substrate, serves as a pattern definer during fabrication of the device and ultimately disappears. The invention thereby offers excellent and simply-effected control over both the doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop with substrate. This aspect of the invention is advantageously enhanced by spacing the source and gate conductive layers vertically apart at a boundary defined by the pattern definer This is done, preferably, by forming a trench in which a source conductive layer is deposited in electrical contact with a doped source region of the substrate at the same time that a gate conductive layer is deposited atop a gate oxide layer. The trench is formed in an exposed portion of the upper surface of the substrate bounded by the pattern definer and gate oxide. In one embodiment, the trench sidewall is profile tailored to