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Hikasa

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(54) **TRENCH-TYPE INSULATED GATE SEMICONDUCTOR DEVICE INCLUDING AN EMITTER TRENCH AND AN OVERLAPPED FLOATING REGION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 166 days.

This patent is subject to a terminal disclaimer.

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CPC H01L 29/4236; H01L 29/7397; H01L 29/6634; H01L 29/402–29/407; H01L 29/7395–29/7398; H01L 29/66333–29/66348
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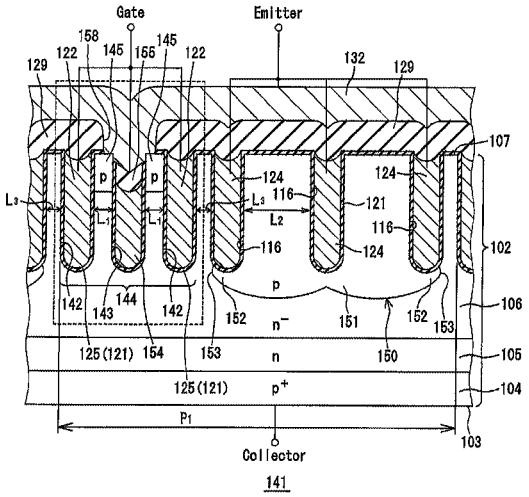
(57) **ABSTRACT**

A semiconductor device includes a semiconductor layer, a plurality of gate trenches, a gate electrode in the plurality of gate trenches, an n^+-type emitter region, a p-type base region, and an n^--type drift region disposed, lateral to each gate trench, a p^+-type collector region, a plurality of emitter trenches formed between the plurality of gate trenches, a buried electrode in the plurality of emitter trenches, and electrically connected with the n^+-type emitter region, and a p-type floating region formed between the plurality of emitter trenches.

17 Claims, 29 Drawing Sheets