in such a way as to impair operation of the selected mode. FIG. **5**, for instance, illustrates an optional switch S**540**, which may be used to disconnect the output of driver X**530** when the regulator circuit is in low-current mode. This ensures that the output impedance of driver X**530** has no effect on the linear regulator control loop operation, and may further minimize wasted current. Of course, other techniques for isolating one control loop from the other may be employed. For instance, driver X**530** may be configured to provide a high-impedance output when not in use.

Because the switching between linear and switching regulator modes is done only when the load current is low, avoiding transient output voltage glitches is straightforward. In some embodiments, changing the gain and/or the DC output level of the error amplifier during the transition may be sufficient. In many embodiments, a capacitor at the output of the regulator (such as C**150**) is sufficiently large that the load can be supported in low-current mode for a short time while the regulator switches modes and stabilizes. In these embodiments, a "soft startup" approach may be used when entering either mode. A soft startup circuit might comprise, in some embodiments, circuitry configured to ensure that the switching transistor begins in the off state, with a duty cycle of zero, upon entry into high-current mode. Similarly, soft startup circuitry may be configured to ensure that the series pass transistor is initialized at a high-resistance state upon entry into low-current mode. Soft startup circuitry may comprise logic and/or analog circuitry configured to change the gain of the shared error amplifier A**125**, in some embodiments, to adjust the feedback ratio, in some embodiments, and/or to temporarily disable or shift the output of error amplifier A**125**, in still other embodiments. Some of these embodiments may include the use of an RC time-constant to adjust the control loop response during a start-up period; in some instances the RC time-constant may be adjustable.

Either or both of multimode regulator circuits **100** and **200**, as well as variations thereof, may be implemented with discrete devices, with one or more integrated circuits, or a combination thereof. In some embodiments, a monolithic integrated circuit or single package may comprise most of the elements described above, with only the inductor L**135** and output capacitor C**150** left "off-chip." In these embodiments, then, a monolithic integrated circuit may comprise a linear regulator sub-circuit configured to supply current to an external load in a low-current mode, responsive to a first control signal from a first control path and a switching regulator sub-circuit configured to supply current to the load in a high-current mode, responsive to a second control signal from a second control path. In these embodiments, the switching regulator sub-circuit may be configured to supply current to the load through an off-chip inductor L**135**. The monolithic integrated circuit may further comprise a shared error amplifier configured to generate an error signal based on the difference between a reference voltage and a feedback signal coupled from the load, as well as a switch configured to selectively route the error signal to the first control path in the low-current mode and to the second control path in the high-current mode. In some embodiments, the integrated circuit's linear regulator sub-circuit and switching regulator sub-circuit may be configured to share a transistor, as described above, so that the shared transistor operates as a variable-resistance pass transistor in the low-current mode and as a low-on-resistance switching transistor in the high-current mode. In these embodiments, current may be supplied to the external load through one or more shared terminals, thus potentially eliminating one or more terminals. Similarly, one or more package pins may be eliminated in implementations where the linear regulator sub-circuit and switching regulator sub-circuit share a transistor and are housed in a single package.

With the above exemplary circuits and their variants in mind, an exemplary method of supplying a current to a load, employing the inventive techniques of the present invention, is illustrated in the process flow diagram of FIG. **4**. In the pictured method, the transitions between low-current and high-current modes are triggered by the detected current—those skilled in the art will appreciate that a nearly identical process may be employed in embodiments where a mode change is signaled by processing logic.

In any event, the pictured process flow of FIG. **4** "begins" at block **410**, with the generation of an error signal, although those skilled in the art will appreciate that several of the pictured "steps" may actually refer to operations that are ongoing during the entire process. Others may be performed continuously during a particular mode.

Thus, for example, the error signal generation of block **410**, which may be performed in some embodiments by comparing a feedback signal derived from a regulator output to a reference voltage, may be performed continuously, in some embodiments. Similarly, block **420** illustrates the comparison of the load current to a threshold value—this operation might also be performed continuously, in some embodiments.

If the current is less than the threshold, the process begins (or continues in) a low-current mode. Thus, the error signal is routed to a linear regulator sub-circuit, as shown at block **430**, and the load current is supplied by the linear regulator, responsive to the error signal, as shown at block **440**. Operation in low-current mode continues until the detected current exceeds the pre-determined threshold (at block **420**), at which time operation switches to high-current mode. The error signal is routed to a switching regulator sub-circuit, as shown at block **450**, and current is supplied to the load, responsive to the error signal, by the switching regulator. Operation in high-current mode continues until a mode change occurs, triggered by a change in current detected at block **420**

With the above range of variations and applications in mind, it should be understood that the present invention is not limited by the foregoing description, nor is it limited by the accompanying drawings. Instead, the present invention is limited only by the following claims, and their legal equivalents.

What is claimed is:

1. A multimode voltage regulator circuit comprising:

a linear regulator sub-circuit configured to supply current to a load in a low-current mode, responsive to a first control signal from a first control path;

a switching regulator sub-circuit configured to supply current to the load in a high-current mode, responsive to a second control signal from a second control path;

a shared error amplifier configured to generate an error signal based on the difference between a reference voltage and a feedback signal coupled from the load; and

a switch configured to selectively route the error signal to the first control path in the low-current mode and to the second control path in the high-current mode.

2. The multimode voltage regulator circuit of claim **1**, wherein the linear regulator sub-circuit and the switching regulator sub-circuit share a transistor, said transistor configured to operate as a variable-resistance pass transistor in the low-current mode and as a low-on-resistance switching transistor in the high-current mode.

3. The multimode voltage regulator circuit of claim **2**, wherein the feedback signal is obtained from a resistive divider network coupled to the load.