INTEGRATED CIRCUIT WITH MULTI-LENGTH OUTPUT TRANSISTOR SEGMENTS

RELATED APPLICATIONS

This application is a continuation of application Ser. No.: 11/799,985 filed May 3, 2007, which is a continuation of application Ser. No.: 11/540,261 filed Sep. 29, 2006, which is a division of application Ser. No.: 10/984,442, filed Nov. 8, 2004, now U.S. Pat. No. 7,135,748, which is a continuation-in-part (CIP) of application Ser. No. 10/974,176 filed Oct. 26, 2004, entitled, "INTEGRATED CIRCUIT WITH A MULTI-LENGTH POWER TRANSISTOR SEGMENTS", each of which is assigned to the assignee of the present application.

FIELD OF THE INVENTION

The present invention relates generally to the field of semiconductor devices; more specifically, to monolithic integrated circuits (ICs) and to methods of manufacturing IC devices.

BACKGROUND OF THE INVENTION

Integrated circuits (ICs), including power integrated circuits (PICs), find application in an increasingly wide variety of electronic devices. Typically, PICs comprise one or more high-voltage field effect transistors (HVFETs) having a device structure such as those disclosed in U.S. Pat. No. 6,207,994 ("the '994 patent"), which is herein incorporated by reference. Each of the devices disclosed in the '994 patent has a source region and a drain region separated by an intermediate region. A gate structure is disposed over a thin oxide layer over the metal-oxide-semiconductor (MOS) channel of the device. In the on state, a voltage is applied to the gate to cause a conduction channel to form between the source and drain regions, thereby allowing current to flow through the device. In the off state, the voltage on the gate is sufficiently low such that no conduction channel is formed in the substrate, and thus no current flow occurs. In this condition, high voltage is supported between the drain and source regions.

Most integrated circuits contain one or more output transistors that control current flow through one or more external loads. By way of example, FIG. 7 of the '994 patent discloses a structure having interdigitated source and drain regions that is commonly utilized as an output transistor in many types of power devices. In the design of a particular PIC, these elongated source/drain segments may be replicated to increase the current handling capability of the power device.

FIG. **1** shows a typical prior art IC fabricated on a semiconductor die **10** having an aspect ratio defined as the ratio of the length (L) to the width (W). Included on semiconductor die **10** is a control circuit **11** that is utilized to control on/off switching of an output transistor **12**. In IC designs, it is customary to utilize a single standardized control circuit design coupled to a variety of output transistor layouts of differing sizes (e.g., number of segments) to create a family of devices with similar functionality, but with differing current handling capability. For example a family of ICs, each with differing current handling capabilities, may be created by increasing the number of parallel segments of transistor **12**. According to this traditional approach, ICs with larger current handling capability have a larger width (W) to accommodate more source/drain segments, but the same length (L). In other words, in prior art IC designs, the length of the output transistor is substantially constant, and equal to the length of control circuit **11**. Integrated circuit devices with more current handling capability have more segments added in parallel, which increases the width of the semiconductor die.

To achieve maximum utilization of the package space that houses semiconductor die **10**, control circuit **11** is usually designed with a length that is much larger than its width. For example, in a typical IC product family the smallest device is designed to be long and narrow (i.e., large aspect ratio), with larger devices having an increased width dimension due to the added number of output transistor segments (i.e., smaller aspect ratio). That is, the aspect ratio of larger devices decreases as more segments are added.

Aspect ratio is a critical parameter in the design of most monolithic ICs, including, by way of example, power integrated circuit devices. An IC fabricated on a semiconductor die having a very large or very small aspect ratio often suffers from mechanical stress caused by the molding compound used to package the die. This stress can adversely change the electrical properties of the IC circuitry. For minimum stress a semiconductor die should have an aspect ratio that is close to 1.0, i.e., a length that is substantially equal to its width. The difficulty, however, is that the output transistors are often required to have elongated segments in order to achieve area efficiency and a specific current handling capability. The package also has maximum cavity size. Thus, while it is desirable to manufacture an IC on a semiconductor die having a substantially square shape, the need to provide a product family with a range of current handling capabilities which fits within a package cavity size has constrained the dimensions of the control circuitry and semiconductor die **10**.

The solution of the prior art has been to provide a control circuit that has a relatively narrow width and a much larger length that is substantially equal to the maximum package cavity size. For example, in FIG. **1** the length of control circuit **11** is about four times its width. However, this causes area inefficiencies due to control circuit wiring. Another significant shortcoming of this prior art approach is that in IC devices with small output field-effect transistors (i.e., fewer segments) suffer from package stress problems caused by high semiconductor die aspect ratio.

Thus, there is an unsatisfied need for an improved monolithic IC design that overcomes the problems of poor control circuit area efficiency and high IC aspect ratio.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description that follows and from the accompanying drawings, which however, should not be taken to limit the invention to the specific embodiments shown, but are for explanation and understanding only.

FIG. **1** shows a circuit layout of a prior art monolithic integrated circuit.

FIG. **2** is circuit layout illustrating an integrated circuit according to one embodiment of the present invention.

FIG. **3** is a circuit schematic diagram that corresponds to the integrated circuit shown in FIG. **2**.

FIG. **4** is circuit layout illustrating an integrated circuit according to another embodiment of the present invention.

FIG. **5** is circuit layout illustrating an integrated circuit according to still another embodiment of the present invention.

FIG. **6** is circuit layout illustrating an integrated circuit according to yet another embodiment of the present invention.