

2. The method of claim 1 wherein said step of secondly determining comprises:

- a) otherwise, determining that said each processor still operating is to continue operations if said each processor's respective view indicates that said processor(s) still operating and still communicatively coupled number(s) more than one-half of said plurality of processors;
- b) otherwise, determining that said each processor still operating is to continue operations if said each processor's respective view indicates that said processor(s) still operating and still communicatively coupled include(s) a predetermined tie-breaker processor; and
- c) otherwise, determining that said each processor still operating is to halt operations.

3. The method of claim 2 wherein before said (b) step of determining, the following step is performed:

otherwise, determining that said each processor still operating is to continue operation if said each processor's respective view indicates that said processor(s) still operating and still communicatively coupled number exactly two and said each processor is said tie-breaker processor.

4. The method of claim 3, further comprising the steps: attempting to determine the state of said tie-breaker processor;

then determining that said each processor still operating is to continue operations if said tie-breaker processor is in a halted or frozen state;

otherwise, determining that said each processor still operating is to continue operations if the state of said tie breaker is indeterminable and said tie breaker is not unreachable; and

otherwise, determining that said each processor still operating is to halt.

5. The method of claim 1 wherein said step of secondly determining further includes:

a) determining that said each processor still operating is to continue operations if said each processor's respective view indicates that said processor(s) still operating and still communicatively coupled number(s) more than one-half of said plurality of processors;

b) otherwise, determining that said each processor still operating is to continue operations if said each processor's respective view indicates that said processor(s) still operating and still communicatively coupled include(s) a predetermined tie-breaker processor; and

c) otherwise, determining that said each processor still operating is to halt operations.

6. The method of claim 1 wherein said step of attempting to firstly determine comprises:

maintaining said each processor's respective view of said multiprocessor system;

communicating said each processor's respective view of said multi-processor system; and preparing to receive respective views of said multi-processor system.

7. The method of claim 6 wherein said step of maintaining includes maintaining a connectivity matrix.

8. The method of claim 6, including the step of updating said connectivity information according to any of said received respective views which are valid.

9. An article of manufacture comprising a computer memory wherein is located a computer program for causing a multi-processor having a plurality of processors communicatively coupled, each of said plurality of processors having a respective memory, to tolerate inter-processor communications faults by

detecting a communications failure;

then attempting to firstly determine on each of said plurality of processors still operating which of said plurality of processors are still operating and still communicatively coupled, thereby determining said each processor's respective view of said multi-processor system;

then secondly determining on said each processor still operating whether said each processor still operating is to halt operations if said each processor's respective view of said multi-processor system indicates that said processor (3) still operating and still communicatively coupled number less than one-half of said plurality of processors; and

then continuing or halting operations on said each processor according to said second determination.

10. A computer system comprising:

a communications network;

a plurality of processors, communicatively connected by means of said network, each of said plurality of processors having a respective memory wherein is located a computer program for causing said computer system to tolerate inter-processor communications faults by detecting a communications failure;

then attempting to firstly determine on each of said plurality of processors still operating which of said plurality of processors are still operating and still communicatively coupled, thereby determining said each processor's respective view of said multi-processor system;

then secondly determining on said each processor still operating whether said each processor still operating is to halt operations if said each processor's respective view of said multi-processor system indicates that said processor(s) still operating and still communicatively coupled number(s) less than one-half of said plurality of processors; and

then continuing or halting operations on said each processor according to said second determination.

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