United States Patent [19]

Furuta

[11] **Patent Number: 4,639,917**

[45] **Date of Patent: Jan. 27, 1987**

[54] **FAULT DETERMINING APPARATUS FOR DATA TRANSMISSION SYSTEM**

[75] Inventor: **Michihiro Furuta**, Hyogo, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **623,705**

[22] Filed: **Jun. 22, 1984**

[30] **Foreign Application Priority Data**

Jun. 24, 1983 [JP] Japan 58-114608

[51] **Int. Cl.**[4] **G06F 11/00**

[52] **U.S. Cl.** **371/16**; 371/10; 371/5; 371/49

[58] **Field of Search** 371/15, 16, 49, 38, 371/10, 5, 18; 364/200, 900

[56] **References Cited**

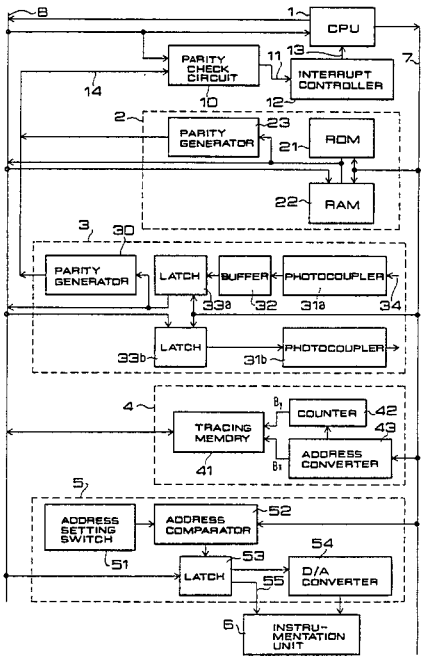
U.S. PATENT DOCUMENTS

3,805,038	4/1974	Buedel	371/18
3,906,200	9/1975	Petschauer	371/10
3,917,933	11/1975	Scheuneman	371/10
3,999,051	12/1976	Petschauer	371/10
4,025,767	5/1977	Bottard	371/16
4,205,370	5/1980	Hirtle	364/200
4,245,344	1/1981	Richter	371/49
4,312,066	1/1982	Bantz	371/16
4,326,291	4/1982	Marsh	371/49
4,371,949	2/1983	Chu	371/38
4,375,664	3/1983	Kim	371/38

Primary Examiner—Michael R. Fleming

Attorney, Agent, or Firm—Bernard, Rothwell & Brown

[57] **ABSTRACT**

A fault-determining apparatus includes parity error checking for data transferred from a main storage and an input/output unit to a CPU which has an interrupt procedure called by the detection of a parity error for recording a parity error signal in a trace recording memory along with a fault-detection signal and data transferred to a data bus from predetermined addresses of interest in the main storage and the input/output unit.

5 Claims, 4 Drawing Figures