

these images are transmitted via a telecommunications network (e.g. via the Internet), the availability of multiresolutional part images creates a difficulty. It is desirable to transmit an image with a reasonable resolution and size quickly which allows the viewer to decide generally on the suitability or correctness of the image. This initial transmission is preferably carried out at a high data compression of the image so as to provide high-speed transmission. Subsequently, the image resolution is preferably increasable selectively, i.e. it should be possible to change the resolution of a local area of the image without introducing artefacts at the borders of the local area and the main image. Dividing the image into blocks and compressing the image using the Discrete Cosine Transform (DCT) provides a method of transmitting a low resolution image quickly, however, the subsequent high fidelity areas may suffer from block artefacts. Using the Discrete Wavelet Transform (DWT) each level of resolution may be transmitted separately. Maximum resolution requires transmitting all the data derived from the image to the destination which has the disadvantage that maximum resolution can only be obtained after waiting for everything to arrive although the method does have the advantage that subsequent image improvement may be carried out at the destination and does not require additional transmissions. No currently available system provides both features: rapid transmission of a low resolution image followed by transmission of a limited amount of data to provide quick and efficient loss-free display of selectable zones of the image.

T. C. Denk, K. K. Parhi describe in an article entitled: "Calculation of minimum number of registers in 2-D discrete wavelet transforms using lapped block processing," *IEEE Int. Symposium on Circuit and Systems*, Vol. 3, pp. 77-80, London, England, May 1994 a technique for minimizing the on-chip memory requirements for the execution of the 2D wavelet transform iterative filtering process in a multi-processor architecture. No indication is given of how to adapt this technique to use less processors than one per level.

Aim of the Invention

It is an object of the present invention to provide a method and apparatus for efficient use of memory and/or memory accesses in the digital filtering of multi-dimensional data structures.

It is a further object of the present invention to provide a method and apparatus for digital filtering of multi-dimensional data structures which requires less processors than one per level.

It is still a further object of the present invention to provide a method and apparatus for digital filtering of multi-dimensional data structures which may be conveniently placed on a single chip.

SUMMARY OF THE INVENTION

The present invention may provide a method of multi-level iterative digital filtering of a data structure, whereby the elements of the data structure form the zero layer in the zero level and the data layer in each subsequent level is given by the results of one iteration, comprising the steps of: subdividing each level into a plurality of regions, there being data dependency between the data in one data layer in one level and the data layers in any other level of a region; filtering each level by lapped-region processing; and scheduling the data processing of each level to provide substantially regional synchronization of the filtering step at each level.

The present invention may also provide a method of multi-level iterative digital filtering of a data structure,

whereby the elements of the data structure form the zero layer in the zero level and the data layer in each subsequent level is given by the results of one iteration, comprising the steps of: subdividing each level into a plurality of regions, there being data dependency between the data in one data layer in one level and the data layers in any other level of a region; filtering each level by lapped-region processing; and selecting the sequence for traversing the regions so that outputs from processing the regions are scheduled to occur at substantially equal time intervals.

The present invention may also provide a method of multi-level iterative digital filtering of a data structure, whereby the elements of the data structure form the zero layer in the zero level and the data layer in each subsequent level is given by the results of one iteration, comprising the steps of: subdividing each level into a plurality of regions, there being data dependency between the data in one data layer in one level and the data layers in any other level of a region; filtering each level by lapped-region processing; stopping the processing at the end of one region; and storing the data related to data dependencies included in adjacent unprocessed regions.

The present invention may also provide a filtering apparatus for multi-level iterative digital filtering of a data structure, whereby the elements of the data structure form the zero level and each subsequent level is defined by the results of one iteration, comprising: a control means for subdividing the data layer of each level into a plurality of regions, there being data dependency between the data in one data layer in one level and the data layers in any other level of a region; a filtering module for filtering each level by lapped-region processing, said filter module being adapted to schedule the data processing of each level to provide substantially regional synchronization of the filtering at each level.

The present invention may also provide a filtering apparatus for multi-level iterative digital filtering of a data structure, whereby the elements of the data structure form the zero level and each subsequent level is defined by the results of one iteration, comprising: a control means for subdividing the data layer of each level into a plurality of regions, there being data dependency between the data in one data layer in one level and the data layers in any other level of a region; a filtering module for filtering each level by lapped-region processing, said filter module being adapted to stop the processing at the end of one region and to store the data relating to data dependencies included in adjacent unprocessed regions.

Each of the above apparatuses may be used in an encoder. Further each of the above apparatuses may include means for individually carrying out any of the method steps of the appended method claims. Lapped regional processing may include zero tree coding.

The present invention may further provide a filtering apparatus for multi-level iterative digital filtering of a multi-level representation of a data structure to reconstruct the data structure, the multi-level representation including data clusters, comprising: a filtering module for filtering the multi-level representation by lapped-cluster processing; a controller for controlling the flow of data through said filtering module, said controller being adapted to schedule the data processing in said filtering module so that substantially only the data which is required for reconstructing a region of the data structure is processed before beginning with the filtering process to reconstruct the next region of the data structure. The apparatus may be used in a decoder. A cluster may be a tree or part of a tree.