95-11 are depicted in an activated disposition that bars removal of active DISK 4, and active DISK 11 from the respective fourth and eleventh bays.

Operation of the logic circuits 110-N and various LEDs used in the present invention will now be described with further reference to FIG. 3, and FIGS. 4A, 4B and 4C. Each logic circuit 110-N includes a resistor R1 (270 Ω in the preferred embodiment), as well as parallel-coupled LED-NA and LED-NB. The anode end of each LED is coupled to the lower end of current limiting resistor R1 and thence to V_{cc}, and the cathode end of each LED is coupled to pins 44 and 74 of the associated SCA connector. (Not shown in FIGS. 4A–4C is a 2 KΩ pull-up resistor connected between V_{cc} and pin 44 inside of each DISK N.) Optional solenoid-like mechanism 95-N is coupled between V_{cc} (or other operating potential) and pin 77 within logic circuit 110-N.

The logic circuits 110-N perform a logical AND operation between the $\overline{\text{MATED}}$ SCA condition and the SCA ACTIVE condition:

$$\text{LIT}=\overline{\text{MATED}}\cdot\text{ACTIVE LED} \quad (1)$$

where MATED=0 denotes grounded pins 44 and 74, and ACTIVE LED=0 denotes grounded pin 77, and LIT=1 denotes lit LEDs.

In FIGS. 2, 3 and 4A, DISK 1 is mated with SCA connector 100-1, but is inactive. As a result, pins 44 and 74 are at ground, and pin 77 is floating. As a consequence, LED1A and LED1B are forward biased and operating current flows from V_{cc}, through R1, the LEDs and to grounded pin 74. With reference to equation (1) above, LIT=$\overline{0}\cdot1=1$, which causes LED1A and LED1B to light steadily. This lit condition signals that operating potential is present in the memory system, and that DISK 1 is mated therein but is presently not active. Because pin 77 is floating, no current flows through mechanism 95-1, and mechanical arm 97 remains in a non-blocking position as also shown in FIG. 3. The LEDs for DISKs 2, 3, 5, 6, 7, 8, 9 and 12 would similarly be steadily lit, and optional mechanisms for these mated but inactive disks would similarly remain unenergized and non-blocking.

Consider now FIG. 4B, in which DISK 4 (like DISK 11) is mated and is active. Mating causes pins 74 and 44 to be ground, which normally would forward bias LED4A and LED4B causing these LEDs to be steadily on or lit. However because disk 4 is active, pin 77 is grounded, typically intermittently as a read/write head within disk unit 4 seeks and then reads or writes data. During such activity, the ground condition at pin 77 diverts current from R1 to grounded pin 77 and away from the LEDs. For as long as pin 77 is ground, the otherwise on LEDs are extinguished. With reference to equation (1) above, LIT=$\overline{0}\cdot0=0$, which extinguishes the LEDs for as long as pin 77 is grounded. However, when pin 77 floats, equation (1) is LIT=$\overline{0}\cdot1=1$, which turns on the LEDs. This off/on flashing continues intermittently as pin 77 typically changes states during storage drive unit activity.

By way of example, if an active period causes pin 77 to be grounded for 500 ms, then ungrounded for 100 ms, then grounded for 1 second, LED4A–LED4B would turn off for 500 ms, turn on for 100 ms, turn off for 1 second, and then turn steadily back on as the active period ended. The result would be a flashing or intermittently lit pair of LEDs, which signals a mated storage unit that is receiving operating power and is presently active. Note that during periods of activity when pin 77 is grounded, mechanism 95-4 is energized causing arm 97 to move from a normally non-blocking position to a position that physically bars removal of active disk 4 from the console rack.

Finally, FIG. 4C depicts an obvious case when an unmated DISK 10 results in no LEDs being lit because there is no connection with connector 100-10. The LEDs are off because their cathodes are floating and there is no current flow path. Similarly, device 95-10 is not energized because the absence of a ground coupled to pin 77 eliminates any current flow path.

FIG. 5 depicts a circuit, here 110-10, used with memory systems 20' that use double memory addressing. In such systems, upper and lower addresses present in the SCSI bus 30, 30' may be used. A switch S10, shown schematically as a single-pole-single-throw switch, responds to high/low addresses available from the SCSI bus via one or more pins on connector 100-10. If upper or high addressing is present, S10 is in the left position shown, and if lower addressing is present, S10 is in the right position. (It is understood that S10 in practice preferably is an electronic switch, rather than a mechanical switch.)

For the high addressing case, shown in FIG. 5, the base of transistor Q10-L is grounded by S10, turning Q10-L off. Thus, regardless of pin conditions at connector 100-10, the cathode end of diodes LED10AL, LED10BL is essentially floating, rendering these LEDs inoperative. However, the base of transistor Q10-H is forward biased through a typically 10 KΩ resistor, turning Q10-H on, producing a relatively low impedance from collector to emitter. This allows diodes LED10AH, LED10BH to be on, off, or intermittent as a function of the various SCA-connector 100-10 pin conditions. If desired, the logical switching functions performed by transistors Q10-L, Q10-H may be performed by substituting logic gates for the transistors, to reduce cost of fabrication.

Modifications and variations may be made to the disclosed embodiments without departing from the subject and spirit of the invention as defined by the following claims.

What is claimed is:

1. A signalling circuit for use with a system that includes a console with at least one bay sized to receive and make electrical connection with a removable electronic unit, the circuit comprising:

a first indicator having a first end coupled to a source of operating potential and having a second end coupled to a first connection in said console that is ground only when a said unit is matingly received and electrically connected to said console;

said first end of said indicator also being coupled to a second connection in said console that is grounded when said unit in matingly received and electrically connected to said console and is in an active state, said second connection being floating otherwise;

wherein when said first connection is not grounded said first indicator is in a first indicating state to indicate an unmated condition between said console and said unit;

wherein when said first connection is grounded and said second connection is floating, said first indicator is in a second indicating state to indicate a mated condition between said console and said unit and to indicate that said unit is presently inactive; and

wherein when said first connection and said second connection are each grounded, said first indicator is in a third indicating state to indicate a mated condition between said console and said unit and to indicate that said unit is presently active.

2. The circuit of claim 1, further including a second indicator, electrically coupled in parallel to said first indicator;