

1

**APPARATUS AND METHODS FOR
FREQUENCY CONTROL IN A
MULTI-OUTPUT FREQUENCY
SYNTHESIZER**

BACKGROUND

Technical Field

The present invention generally relates to the field of communications, and more particularly relates to techniques for generating and controlling precision frequency sources in cellular telephones or other communications devices.

Background

Modern communications devices, whether communicating via a wire or wirelessly, typically require at least one clock operating at a relatively stable reference frequency. With increased integration, devices such as cellular phones now commonly include additional communication functions such as wireless local-area network (W-LAN) transceivers, Bluetooth radios, Global Positioning System (GPS) receivers, Universal Serial Bus (USB) interfaces, and so on. In addition, cellular standards are becoming more complex, with a trend towards the simultaneous use of multiple communications channels, each of which may use a different operating frequency.

Each communication block needs one or more clock frequencies, whether for clocking baseband circuitry or digital signal processors, or for use as local oscillators in radio circuitry. The exact operating frequencies required for each block may vary, and the accuracy requirements may also vary from one function to the next. For instance, a cellular phone typically must have local oscillators that are accurate to about 0.1 parts-per-million (ppm) with respect to a reference at the base station receiving the phone's transmissions. Since Doppler shift caused by a phone's motion relative to the base station can cause an apparent frequency shift of up to 0.5 ppm, this accuracy is typically achieved through the use of well-known Automatic Frequency Control (AFC) techniques. A GPS receiver, on the other hand, will work quite well with frequency accuracies on the order of 0.5 ppm, or even 2 or 3 ppm, but may require that its frequency reference be stable to within 2 parts-per-billion (ppb) for the duration of a measurement interval for best performance. In contrast, a Bluetooth radio may only require reference frequency accuracies on the order of 20 ppm.

To minimize costs, devices may share a reference clock. For instance, U.S. Pat. No. 6,867,734 to Voor et al. describes a communications device combining a cellular transceiver and a GPS receiver, in which a shared reference clock is used to synthesize a local oscillator signal for the communications transceiver and a high-frequency clock signal for the GPS receiver. However, sharing a reference clock can cause several problems.

First, if AFC is used to adjust the reference clock frequency so that, for example, a cellular transceiver local oscillator (LO) tracks the frequency of a received base station signal, then changes in the reference clock frequency are reflected in other circuits sharing the reference. A temporary loss of the received signal, such as may occur when driving through a tunnel, may cause unexpected variations in the reference clock frequency due to the AFC loop's response to the loss of signal. These variations may impair performance in other circuits sharing the reference. Changes to the reference frequency due to tracking Doppler errors will also be passed

2

through to other circuits sharing the reference clock, again causing possible performance impairments. Furthermore, AFC corrections to the reference clock frequency, even if relatively small, may disrupt performance in applications that require clock stability during a critical interval.

In view of the foregoing, disclosed herein are methods and apparatus for generating, from a single reference clock signal, two or more clock signals for separate applications in a communications device.

SUMMARY

The teachings presented herein provide methods and circuits for synthesizing two or more signals phase-locked to a common reference frequency signal. In several embodiments, a method comprises generating first and second output signals phase-locked to a reference clock signal, using first and second phase-locked loop circuits. In response to a detected frequency error in the first output signal, the first output signal is corrected by adjusting a frequency-division ratio in the first phase-locked loop circuit. The second output signal is corrected, separately from the correction to the first output signal, by adjusting a frequency-division ratio in the second phase-locked loop circuit, using an adjustment parameter calculated from the detected frequency error.

In another exemplary method, first and second output signals are generated as described above, using first and second phase-locked loop circuits. The first output signal is corrected by adjusting a frequency-division ratio in the first phase-locked loop circuit and generating a control signal to adjust the frequency of the reference clock signal, in response to detected frequency error in the first output signal. Because the second output signal is derived from the common reference clock signal, adjustments to the reference clock frequency will also adjust the frequency of the second output signal. Additional adjustments to the second output signal may be applied in some embodiments by adjusting a frequency-division ratio in the second phase-locked loop circuits.

A frequency synthesizer circuit according to one or more embodiments of the present invention comprises first and second phase-locked loop circuits configured to generate first and second output signals, respectively, each output signal phase-locked to a common reference clock signal. The frequency synthesizer circuit further comprises a frequency correction circuit configured to correct the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit, in response to a detected frequency error in the first output signal. The frequency correction circuit is further configured to calculate an adjustment parameter, based on the detected frequency error, and to correct the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

In several embodiments, the frequency correction circuit is configured to calculate the adjustment parameter based on an offset, so that the first and second output signal frequencies are corrected in different proportions. In one or more embodiments, the frequency correction circuit is configured to schedule the adjustments applied to any or all of the first or second frequency-division ratios or to the reference clock, to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

An exemplary communications device is also disclosed, comprising a communications transceiver circuit, a second receiver circuit, a first and second phase-locked loop circuits configured to generate first and second output signals, respec-