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(54) **APPARATUS AND METHODS FOR FREQUENCY CONTROL IN A MULTI-OUTPUT FREQUENCY SYNTHESIZER**

FOREIGN PATENT DOCUMENTS

EP	1206039	A2	5/2002
WO	03/098258	A1	11/2003
WO	20061031672		3/2006
WO	2008/021810	A2	2/2008

* cited by examiner

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,132,633	A *	7/1992	Wong et al.	327/113
5,313,346	A *	5/1994	Shimotashiro et al.	360/77.13
5,572,167	A *	11/1996	Alder et al.	331/2
6,236,703	B1	5/2001	Riley	
6,856,791	B2	2/2005	Klemmer	
6,867,734	B2	3/2005	Voor et al.	
2003/0176173	A1 *	9/2003	Klemmer	455/182.2
2003/0214432	A1	11/2003	Tawadrous et al.	
2003/0214436	A1	11/2003	Voor et al.	
2003/0219082	A1 *	11/2003	Tanaka et al.	375/324
2005/0078743	A1 *	4/2005	Shohara	375/219
2006/0215778	A1	9/2006	Murthy et al.	
2009/0258657	A1 *	10/2009	Tanaka et al.	455/456.1

(57) **ABSTRACT**

Methods and circuits for synthesizing two or more signals phase-locked to a common reference frequency signal are disclosed. In one embodiment, a method comprises generating first and second output signals phase-locked to a reference clock signal, using first and second phase-locked loop circuits. In response to a detected frequency error in the first output signal, the first output signal is corrected by adjusting a frequency-division ratio in the first phase-locked loop circuit. The second output signal is corrected, separately from the correction to the first output signal, by adjusting a frequency-division ratio in the second phase-locked loop circuit, using an adjustment parameter calculated from the detected frequency error. In another exemplary method, first and second output signals are generated as described above, using first and second phase-locked loop circuits. The first output signal is corrected by adjusting a frequency-division ratio in the first phase-locked loop circuit and generating a control signal to adjust the frequency of the reference clock signal, in response to detected frequency error in the first output signal. Because the second output signal is derived from the common reference clock signal, adjustments to the reference clock frequency will also adjust the frequency of the second output signal. Additional adjustments to the second output signal may be applied in some embodiments by adjusting a frequency-division ratio in the second phase-locked loop circuits. Circuits for implementing the described methods are also disclosed.

25 Claims, 5 Drawing Sheets

