conductor devices **710**(*a–i*) of the present invention. The nine devices **710**(*a–i*) are arranged in a plurality of rows and columns. A plurality of control signals **60**(*a–c*) access each device **710** in the same column. Each device **710** comprises a semiconductor die **16** without an ESD circuit integrated therewith. In the preferred embodiment, the integrated circuit die **16** is a DDR (DRAM) memory device. However, the present invention is not so limited and can be any type of device that requires operation at a high transmission rate. The die **16** is packaged along with a separate ESD circuit **22**, such as a schottkey diode **22**, in a package **30**, in the manner described heretofore. The package **30** receives an external lead **20** and is connected to the schottkey diode **22** and to the bonding pad **24** (not shown) of the die **16**. In addition, however, the device **710** also comprises a resistor **36**, connected in series with the external lead **20**, and which is switchably connected by switch **32***b* to the bonding pad **24**. The resistor **36** can be made of a thin film resistor and can be very precise. In a preferred embodiment, the resistor **36** has 50Ω resistance. The switch **32***b* can be controlled by the control signal **60***c* supplied along the column line. Therefore, the switch **32***b* can be a transistor which can be electrically activated. In addition, the external lead **20** is supplied along a parallel path to a second switch **32***a*, which is activated by a signal from the control line **64***c*. If the switch **32***a* is activated, the signal from the external lead **20** is supplied directly to the bonding pad **24**. The external leads **20** to each device **710** in the same row are all connected to the same row signal line **62**.

Referring to FIG. **8***b*, there is shown a schematic circuit drawing of another embodiment of a plurality of packaged devices **710** of the present invention. Similar to the devices **710** shown in FIG. **8***a*, the devices **710** shown in FIG. **8***b* are arranged in a plurality of rows and columns. The only difference between the embodiment shown in FIG. **8***b* and that shown in FIG. **8***a* is that the external lead **20** for each device **710** is individually supplied with the signal supplied on signal line **62**(*a–i*), and is not supplied in common to the same row.

What is claimed is:

1. A method of bonding a semiconductor die without an ESD circuit and a separate ESD circuit to an external lead, said method comprising:

bonding said external lead to said separate ESD circuit;

then bonding said separate ESD circuit to said semiconductor die;

packaging said die and said circuit in a single package, wherein said external lead is bonded to said ESD circuit and to said semiconductor die

coupling the package to a chip carrier, said carrier having a first surface having said external lead, and a second surface opposite said first surface and an aperture between said first surface and said second surface

said semiconductor die having a mounting surface with a mounting pad thereon;

said mounting surface facing said second surface with said mounting pad in said aperture;

said ESD circuit on said mounting surface in said aperture;

wherein said external lead is bonded to said ESD circuit in said aperture and to said mounting pad in said aperture; and

wherein said semiconductor die is a memory die, said die being substantially rectilinear in share with a plurality of rows having a plurality of mounting pads thereon substantially in the middle of said rectilinear shape.

2. The method of claim **1**, wherein a plurality of ESD circuits are mounted on a strip.

3. The method of claim **2** further comprising mounting said strip of ESD circuits to said mounting surface of said semiconductor die, adjacent to said plurality of mounting pads prior to bonding an external lead to one of said ESD circuits.

4. A semiconductor device comprising:

a chip carrier having a first surface having a plurality of leads, and a second surface opposite said first surface and an aperture between said first surface and said second surface;

a semiconductor die having a mounting surface with a mounting pad thereon, wherein said die is substantially rectilinearly shaped with a plurality of rows of mounting pads substantially in the middle of said die;

said mounting surface facing said second surface with said mounting pad in said aperture;

an ESD circuit on said mounting surface in said aperture;

a first electrical connector connecting one of said plurality of leads to said ESD circuit; and

a second electrical connector connecting said ESD circuit to said mounting pad, wherein said first electrical connector and said second electrical connector are the same connector.

5. The semiconductor device claim **4** further comprising:

a die adhesive for attaching said semiconductor die to said chip carrier; and

a package for encapsulating said ESD circuit and said aperture.

6. The semiconductor device of claim **5** wherein said package further encapsulates said die with said chip carrier.

7. The semiconductor device of claim **4** further comprising a plurality of ESD circuits, each mounted on said mounting surface with each ESD circuit substantially adjacent to a mounting pad in said aperture.

8. A method of assembling a semiconductor device, said device including a semiconductor die having an integrated circuit with a plurality of rows of mounting pads connecting to said integrated circuit, on a mounting surface, said method comprising:

mounting a strip on said mounting surface, substantially adjacent to said plurality of rows of mounting pads, said strip having a plurality of ESD circuits;

bonding an external lead to one of said ESD circuits; and

then bonding one of said ESD circuits having said external lead bonded, to one of said mounting pads.

9. The method of claim **8** further comprising the step of:

mounting said semiconductor die on a chip carrier, said chip carrier having a first surface with a plurality of external leads, a second surface, opposite said first surface, and an aperture between said first surface and said second surface; said die mounted with said mounting surface facing said second surface and said mounting pads in said aperture.

10. The method of claim **9** wherein said semiconductor die is mounted on said chip carrier before said strip is mounted on said die.

11. The method of claim **9** wherein said semiconductor die with said strip mounted thereon is mounted on said chip carrier with said ESD circuits in said aperture.

12. The method of claim **9** wherein said external lead is bonded to one of said ESD circuits and said same external lead is bonded to one of said mounting pads.

13. The method of claim **4** wherein said integrated circuit is a circuit.