METHOD OF BONDING A SEMICONDUCTOR DIE WITHOUT AN ESD CIRCUIT AND A SEPARATE ESD CIRCUIT TO AN EXTERNAL LEAD, AND A SEMICONDUCTOR DEVICE MADE THEREBY

This non-provisional application claims the priority of a Provisional Application Ser. No. 60/358,117 filed on Feb. 20, 2002 and a Provisional Application Ser. No. 60/380,033 filed on May 6, 2002, whose disclosures are incorporated herein in their entirety by reference.

TECHNICAL FIELD

The present invention relates to a method of bonding a semiconductor die without an ESD circuit and a separate ESD circuit to an external lead, and more particularly to a semiconductor device made thereby.

BACKGROUND OF THE INVENTION

In a semiconductor device, which has a semiconductor die having an integrated circuit thereon, it is well known to have an ESD circuit to protect the input/output signal of the integrated circuit from electrostatic discharge. Typically, the ESD circuit is integrated with the integrated circuit onto the same single semiconductor die.

In U.S. Pat. Nos. 6,198,136 and 6,066,890, the references disclose the ESD circuit being a separate circuit apart from a semiconductor die and packaged together in a single package to protect and enhance the performance of the integrated circuit die. See, for example, FIGS. **3–5** and column 3, lines 29–50 of U.S. Pat. No. 6,066,890. However, one of the shortcomings of these references is that the particular order by which the external leads are bonded or connected to the various circuits is not disclosed. This is important in that since the ESD circuit is removed from the integrated circuit die, the die is "exposed" to the harmful effects of ESD, during the bonding process.

Further, the references do not disclose particular structures of chip carriers and semiconductor dies that may be connected to the separate ESD circuit advantageously. In particular, such a structure would be useful for packaging a semiconductor die with the integrated circuit as memory circuits. Finally, the references do not disclose the use of separate ESD circuits with terminating resistors outside of the semiconductor die but part of the package of the semiconductor device. These and other shortcomings are overcome by the present invention.

Other relevant art includes U.S. Pat. Nos. 5,771,140; 6,385,021; and 5,859,758.

SUMMARY OF THE INVENTION

In the present invention, a method for bonding a semiconductor die without an ESD circuit and a separate ESD circuit to an external lead is disclosed. In the method of the present invention, the external lead is first bonded to the separate ESD circuit. Thereafter, the separate ESD circuit with the external lead bonded thereto is then bonded to the semiconductor die.

The present invention also relates to a semiconductor device which has a chip carrier, a semiconductor die, and an ESD circuit. The chip carrier has a first surface with a plurality of leads and a second surface opposite to the first surface, and an aperture between the first surface and the second surface. The semiconductor die has a mounting surface with a mounting pad thereon facing the second surface with the mounting pad in the aperture. The ESD circuit is on the mounting surface in the aperture. A first electrical connector connects one of the plurality of leads to the ESD circuit and a second electrical connector connects the ESD circuit to the mounting pad.

In addition, the present invention relates to a method of assembling a semiconductor device wherein a strip containing a plurality of ESD circuits is mounted on the mounting surface of the semiconductor die with the strip containing a plurality of ESD circuits mounted substantially adjacent to a plurality of rows of mounting pads of the semiconductor die.

Finally, the present invention relates to a semiconductor device which has a semiconductor die with an input pad, an ESD circuit electrically connected to the input pad, and a terminating resistor switchably connected to the input pad. The ESD circuit and the resistor are external to the die, but packaged in the same package. An external lead is connected to the input pad.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a top view of a first embodiment of an unpackaged semiconductor device manufactured by the method of the present invention, with FIG. **1**B being a cross-sectional view of the device shown in FIG. **1**A.

FIG. **2**A is a top view of a second embodiment of an unpackaged semiconductor device manufactured by the method of the present invention, with FIG. **2**B being a cross-sectional view of the device shown in FIG. **2**A.

FIG. **3**A is a top view of a third embodiment of an unpackaged semiconductor device manufactured by the method of the present invention, with FIG. **3**B being a cross-sectional view of the device shown in FIG. **3**A.

FIG. **4**A is a top view of a fourth embodiment of an unpackaged semiconductor device manufactured by the method of the present invention, with FIG. **4**B being a cross-sectional view of the device shown in FIG. **4**A.

FIG. **5**A is a top view of a fifth embodiment of an unpackaged semiconductor device manufactured by the method of the present invention, with FIG. **5**B being a cross-sectional view of the device shown in FIG. **5**A.

FIG. **6**A is a top view of a sixth embodiment of an unpackaged semiconductor device of the present invention, also made by the method of the present invention, with FIG. **6**B being a cross-sectional view of the device shown in FIG. **6**A.

FIGS. **7***a* & **7***b* are schematic circuit diagrams of a plurality of semiconductor devices of the present invention each packaged with a terminating resistor switchably connectable by a control signal.

FIGS. **8***a* & **8***b* are schematic circuit diagrams of a plurality of semiconductor devices of the present invention, each packaged with a series resistor switchably connectable by a first control signal and a second control signal.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**A and FIG. **1**B there is shown a top view of an unpackaged semiconductor device **10** made in accordance with the method of the present invention. The device **10** comprises a semiconductor die or an integrated circuit chip **16**. The chip **16** is typically substantially rectangular in shape having I/O pads **24** around the periphery or the perimeter thereof. The chip **16** can be any type of