

In another embodiment of the bond pad structure **50**, the bond pad **47** may be placed on the substrate **7** along with, for example, device **10**, for example, a coplanar waveguide, thermocouples **30**, first circuit **32**, and second circuit **34**, for example, detection and output circuitry. In this embodiment, the substrate **7** may be etched in two steps, as illustrated in FIGS. **6A**, **6B**, **7A**, and **7B**. Thus, a single cavity **45** may be formed suspending the bond pad **47**, device **10**, thermocouples **30**, first circuit **32**, and second circuit **34**. While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiment, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A method of manufacturing a low-loss microwave power sensor device, comprising the steps of:
 - providing a semiconductor substrate having an upper and a lower surface, said upper surface having thereon a layer of an etch-resistant material;
 - providing a co-planar microwave waveguide on a portion of said substrate upper surface, said co-planar waveguide including a pair of spaced-apart, elongated ground conductors and an elongated signal conductor in the space between said ground conductors and a pair of resistive elements at one end of said ground and signal conductors;
 - providing a thermopile assembly comprising at least a pair of thermocouple sensor elements on another portion of said substrate upper surface facing said pair of resistive elements at a spacing therefrom;
 - forming a pattern of spaced-apart openings in said etch-resistant layer on said substrate upper surface, said pattern defining length and width dimensions and location of a cavity to be formed within a portion of said substrate upper surface;

etching said substrate upper surface through said openings in said etch-resistant layer with a first etchant to form a plurality of partial cavities therein, each having dimensions less than said length and width dimensions; and etching said substrate upper surface through said openings in said etch-resistant layer with a second etchant to complete formation of said cavity,

wherein the dimensions and substrate portion of said cavity are selected such that said cavity is positioned beneath said elongated ground and signal conductors of said waveguide and beneath the portion of said thermopile assembly in spaced adjacency to said resistive elements of said waveguide, whereby the resistive elements of said waveguide and said thermocouple sensor elements of said thermopile assembly overhang said cavity in spaced adjacency.

2. The method according to claim **1**, wherein the etching of said cavity using the first and second etchants includes etching the top surface portion of the substrate from directly beneath the waveguide and thermopile assembly after providing each on said substrate portions.

3. The method according to claim **1**, wherein said first etchant is an isotropic etchant and said second etchant is an anisotropic etchant.

4. The method according to claim **3**, wherein said semiconductor substrate comprises silicon, said first, isotropic etchant comprises xenon difluoride (XeF_2), and said second, anisotropic etchant comprises ethylenediamine-pyrocatechol-water.

5. The method according to claim **4**, further comprising providing detection and output circuitry on yet another portion of said substrate upper surface.

6. The method according to claim **1**, comprising providing said pattern of openings in said etch-resistant layer in parallel with the length and width dimensions of said ground and signal conductors of said waveguide.

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