US009543408B1

(12) **United States Patent**
**Lin et al.**

(10) **Patent No.: US 9,543,408 B1**
(45) **Date of Patent: Jan. 10, 2017**

(54) **METHOD OF FORMING PATTERNED HARD MASK LAYER**

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( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/835,730**

(22) Filed: **Aug. 26, 2015**

(51) **Int. Cl.**

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|---|---|
| ***H01L 21/3205*** | (2006.01) |
| ***H01L 29/66*** | (2006.01) |
| ***H01L 21/02*** | (2006.01) |
| ***H01L 21/265*** | (2006.01) |
| ***H01L 21/324*** | (2006.01) |
| ***H01L 21/3213*** | (2006.01) |
| ***H01L 21/3215*** | (2006.01) |

(52) **U.S. Cl.**
CPC ... ***H01L 29/66545*** (2013.01); ***H01L 21/02532*** (2013.01); ***H01L 21/02592*** (2013.01); ***H01L 21/26513*** (2013.01); ***H01L 21/324*** (2013.01); ***H01L 21/32055*** (2013.01); ***H01L 21/32139*** (2013.01); ***H01L 21/32155*** (2013.01); ***H01L 29/66795*** (2013.01)

(58) **Field of Classification Search**
CPC ..... H01L 21/02592; H01L 21/02532; H01L 21/0257; H01L 21/02675; H01L 21/02686; H01L 21/0268; H01L 29/66409; H01L 23/544; G03F 9/7084
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

| | | | | |
|---|---|---|---|---|
| 6,008,098 | A * | 12/1999 | Pramanick | H01L 21/26506 257/E21.335 |
| 8,111,376 | B2 | 2/2012 | Adel | |
| 8,188,447 | B2 | 5/2012 | Yang | |
| 2003/0042484 | A1* | 3/2003 | Horikoshi | H01L 29/4908 257/48 |
| 2008/0316442 | A1 | 12/2008 | Adel | |
| 2012/0190216 | A1* | 7/2012 | Chan | H01L 21/82341 438/799 |
| 2014/0356982 | A1 | 12/2014 | Barash | |
| 2015/0060970 | A1* | 3/2015 | Sasaki | H01L 27/10855 257/296 |
| 2015/0270373 | A1* | 9/2015 | Horak | H01L 29/66545 257/401 |
| 2016/0181381 | A1* | 6/2016 | Liu | H01L 29/41783 257/401 |

* cited by examiner

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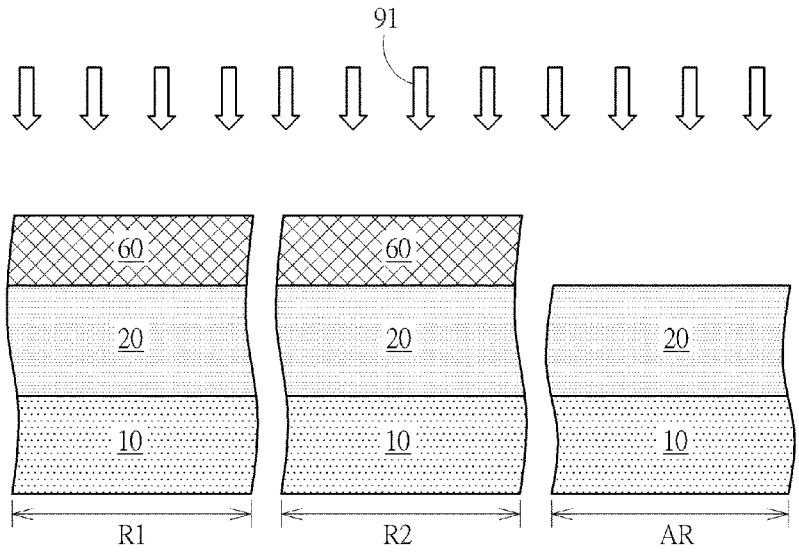
(57) **ABSTRACT**

A method of forming a patterned hark mask layer includes the following steps. A semiconductor substrate is provided. An amorphous silicon layer is formed on the semiconductor substrate. An implantation process is performed on the amorphous silicon layer. An annealing treatment is performed on the amorphous silicon layer after the implantation process. A patterned hard mask layer is formed on the amorphous silicon layer after the annealing treatment.

**12 Claims, 5 Drawing Sheets**