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(54) **STRUCTURE AND METHOD FOR OVERLAY MARKS**

(75) Inventors: **Hsien-Cheng Wang**, Hsinchu (TW); **Ming-Chang Wen**, Kaohsiung (TW); **Chun-Kuang Chen**, Hsinchu (TW); **Yao-Ching Ku**, Hsinchu (TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.** (TW)

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G03F 7/20	(2006.01)
H01L 29/51	(2006.01)

(52) **U.S. Cl.**

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(58) **Field of Classification Search**

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USPC 438/16, 401, 462, 17, 14; 257/797, 257/E23.179

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

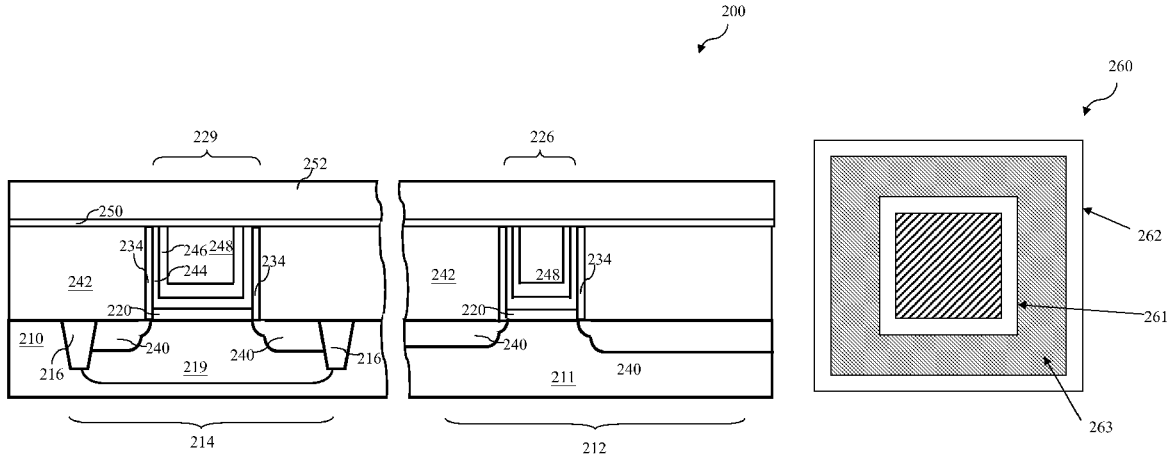
8,163,572	B2 *	4/2012	Hashimi	H01L 22/12 257/368
2002/0009824	A1 *	1/2002	Maeda	438/80
2006/0060904	A1	3/2006	Hong	
2007/0138561	A1 *	6/2007	Hashimi et al.	257/368
2008/0237661	A1 *	10/2008	Ranade et al.	257/288
2009/0090982	A1 *	4/2009	Ranade et al.	257/408
2009/0098696	A1 *	4/2009	Lin et al.	438/238
2010/0052060	A1 *	3/2010	Lai et al.	257/368
2010/0059833	A1 *	3/2010	Yu	H01L 21/82380 257/410
2010/0117154	A1 *	5/2010	Ye	H01L 21/26513 257/368
2011/0254054	A1 *	10/2011	Itou	H01L 21/26506 257/192
2011/0284966	A1 *	11/2011	Wen et al.	257/368
2011/0285036	A1 *	11/2011	Yao et al.	257/797
2012/0038021	A1 *	2/2012	Chen et al.	257/506
2013/0330904	A1 *	12/2013	Yao	G03F 7/70633 438/401

* cited by examiner

Primary Examiner — Latanya N Crawford

(74) *Attorney, Agent, or Firm* — Hauptman Ham, LLP

(57) **ABSTRACT**

The overlay mark and method for making the same are described. In one embodiment, a semiconductor overlay structure includes gate stack structures formed on the semiconductor substrate and configured as an overlay mark, and a doped semiconductor substrate disposed on both sides of the gate stack structure that includes at least as much dopant as the semiconductor substrate adjacent to the gate stack structure in a device region. The doped semiconductor substrate is formed by at least three ion implantation steps.

20 Claims, 11 Drawing Sheets