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(54) **METHOD FOR REDUCING POWER CONSUMPTION IN SOLID-STATE STORAGE DEVICE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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See application file for complete search history.

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(57) **ABSTRACT**

Apparatus and methods of reducing power consumption in solid-state storage devices such as solid-state disks (SSDs) that can reduce idle power levels in an SSD, while maintaining low resume latency upon exiting a reduced power state. By arranging a storage controller and at least one NAND flash package of the SSD in separate power islands, storing context information for the SSD in at least one page buffer of NAND flash memory within the NAND flash package on one power island upon entering the reduced power state, and, once the context information is stored in the page buffer, allowing the NAND flash memory to enter a standby mode, placing the storage controller on the other power island in a predefined low power mode, and removing power from any unneeded components on the same power island as the storage controller, a scalable approach to reducing idle power levels in the SSD can be achieved.

17 Claims, 6 Drawing Sheets