vertical direction; a second P-type lightly doped diffusion (PLDD) region, which is formed on the second P-well in the epitaxial layer, and is located between the epitaxial top surface and the second P-well in the vertical direction; a P-type source, which is formed on the second N-well in the epitaxial layer, and is located between the epitaxial top surface and the second N-well in the vertical direction, wherein the P-type source connects the N-type body region and the second NLDD region in the lateral direction; a P-type drain, which is formed on the second P-well in the epitaxial layer, and is located between the epitaxial top surface and the second P-well in the vertical direction, wherein the P-type drain connects the second PLDD region in the lateral direction; and a separation region, which is connected between the PMOS device region and the NMOS device region, for separating the PMOS device region and the NMOS device region, wherein a depth of the separation region, which is measured from the epitaxial top surface downward, is not smaller than a depth of any of the first P-well, the first N-well, the second N-well, and the second P-well; wherein, the first PN junction is located between the first PLDD region and the first NLDD region; wherein, the second PN junction is located between the second PLDD region and the second NLDD region.

In one perspective, the present invention also provides a manufacturing method of a dual-well complementary metal oxide semiconductor (CMOS) device. The manufacturing method includes: providing a substrate, which includes a top surface and a bottom surface opposite to the top surface in a vertical direction; forming an epitaxial layer on and connecting at least a portion of the top surface of the substrate, the epitaxial layer including an epitaxial top surface opposite to the top surface in the vertical direction; forming an isolation region on the epitaxial layer, to define an NMOS device region and a PMOS device region in the epitaxial layer; forming a first P-type well (P-well) in the NMOS device region of the epitaxial layer, under the epitaxial top surface in the vertical direction; forming a P-type body region on the first P-well in the epitaxial layer, between the first P-well and the epitaxial top surface in the vertical direction; forming a first N-type well (N-well) in the NMOS device region of the epitaxial layer, under the epitaxial top surface in the vertical direction, wherein the first N-well connects the first P-well in a lateral direction, to form a first PN junction between the first N-well and the first P-well; forming a first gate in the NMOS device region, wherein the first gate is stacked on and connects the epitaxial top surface in the vertical direction; forming a first P-type lightly doped diffusion (PLDD) region on the first P-well in the epitaxial layer, between the epitaxial top surface and the first P-well in the vertical direction; forming a first N-type lightly doped diffusion (NLDD) region on the first N-well in the epitaxial layer, between the epitaxial top surface and the first N-well in the vertical direction; forming an N-type source on the first P-well in the epitaxial layer, between the epitaxial top surface and the first P-well in the vertical direction, wherein the N-type source connects the P-type body region and the first PLDD region in the lateral direction; forming an N-type drain on the first N-well in the epitaxial layer, between the epitaxial top surface and the first N-well in the vertical direction, wherein the N-type drain connects the first NLDD region in the lateral direction; forming a second N-type well (N-well) in the PMOS device region of the epitaxial layer, under the epitaxial top surface in the vertical direction; forming an N-type body region on the second N-well in the epitaxial layer, between the second N-well and the epitaxial top surface in the vertical direction; forming a second P-type well (P-well) in the PMOS device region of the epitaxial layer, under the epitaxial top surface in the vertical direction, wherein the second P-well connects the second N-well in a lateral direction, to form a second PN junction between the second N-well and the second P-well; forming a second gate in the PMOS device region, wherein the second gate is stacked on and connects the epitaxial top surface in the vertical direction; forming a second N-type lightly doped diffusion (NLDD) region on the second N-well in the epitaxial layer, between the epitaxial top surface and the second N-well in the vertical direction; forming a second P-type lightly doped diffusion (PLDD) region on the second P-well in the epitaxial layer, between the epitaxial top surface and the second P-well in the vertical direction; forming a P-type source on the second N-well in the epitaxial layer, between the epitaxial top surface and the second N-well in the vertical direction, wherein the P-type source connects the N-type body region and the second NLDD region in the lateral direction; forming a P-type drain on the second P-well in the epitaxial layer, between the epitaxial top surface and the second P-well in the vertical direction, wherein the P-type drain connects the second PLDD region in the lateral direction; and forming a separation region, which is connected between the PMOS device region and the NMOS device region, for separating the PMOS device region and the NMOS device region, wherein a depth of the separation region, which is measured from the epitaxial top surface downward, is not smaller than a depth of any of the first P-well, the first N-well, the second N-well, and the second P-well; wherein, the first PN junction is located between the first PLDD region and the first NLDD region; wherein, the second PN junction is located between the second PLDD region and the second NLDD region.

In one preferable embodiment, the isolation region includes a local oxidation of silicon (LOCOS) structure or a shallow trench isolation (STI) structure.

In one preferable embodiment, an impurity concentration of the first PLDD region is higher than an impurity concentration of the first P-well, and an impurity concentration of the first NLDD region is higher than an impurity concentration of the first N-well.

In one preferable embodiment, an impurity concentration of the second PLDD region is higher than an impurity concentration of the second P-well, and an impurity concentration of the second NLDD region is higher than an impurity concentration of the second N-well.

In one preferable embodiment, the CMOS device further includes an N-type buried layer, which is formed at or around an interface between the substrate and the epitaxial layer, the N-type buried layer upwardly connecting the second P-well in the vertical direction.

In one preferable embodiment, the separation region includes a deep trench isolation (DTI) structure.

In one preferable embodiment, the separation region includes: a P-type separation region, which is formed in the NMOS device region of the epitaxial layer, the P-type separation region upwardly connecting the epitaxial top surface in the vertical direction, and the P-type separation region laterally connecting the first N-well in the lateral direction; and an N-type separation region, which is formed in the PMOS device region of the epitaxial layer, the N-type separation region upwardly connecting the epitaxial top surface in the vertical direction, and the N-type separation region laterally connecting the second P-well in the lateral direction.