detailed description, some processing steps or operations that are known in the art may have been combined together for presentation and for illustration purposes and in some instances may have not been described in detail. In other instances, some processing steps or operations that are known in the art may not be described at all. It should be understood that the following description is rather focused on the distinctive features or elements of various embodiments of the present invention.

The present invention generally relates to semiconductor device manufacturing, and more particularly to the fabrication of III-V fins and IV fins having a similar fin pitch and on a shared surface. Ideally, it may be desirable to form III-V fins and IV fins having a similar fin pitch and on a shared surface without the need for long epitaxial growth times and with low levels of defects. The purpose of forming III-V fins and IV fins having a similar fin pitch and on a shared surface may be to allow circuit designers to follow the design rule, as is known in the art.

One way to form III-V fins and IV fins having a similar fin pitch and on a shared surface is to form the IV fins in a pFET region and an nFET region, form a spacer layer on the IV fins, remove the spacer layer from a top surface and a side surface of the IV fins in the nFET region, form the III-V fins on the top surface and the side surface of the IV fins in the nFET region, remove the IV fins from the nFET region, and remove the spacer layer from both the pFET and nFET regions. One embodiment by which to form III-V fins and IV fins having a similar fin pitch and on a shared surface is described in detail below with reference to the accompanying drawings FIGS. **1-11**. It should be noted, the present embodiment utilizes the III-V group and IV group semiconductors but other materials may be used. Additionally, IV fins may be referred to as first fins and the III-V fins may be referred to as second fins.

Referring now to FIGS. **1** and **2**, demonstrative illustrations of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface are provided, according to an exemplary embodiment. More specifically, the method can start with fabricating mandrels **106** in a substrate.

The substrate may be any substrate known in the art, such as, for example, a semiconductor-on-insulator (SOI) substrate or a bulk substrate. In an embodiment, an SOI substrate is used. The SOI substrate includes a semiconductor layer **105**, a buried insulator layer **104**, and a base substrate **102**. The semiconductor layer **105** is on the buried insulator layer **104** and the buried insulator layer **104** is on the base substrate **102**. The SOI substrate may be formed using any technique known in the art, such as, for example, Separation by Ion Implantation of Oxygen (SIMOX) or a layer transfer process. When a layer transfer process is employed, an optional thinning step may follow the bonding of two semiconductor wafers together. The optional thinning step can reduce the thickness of a layer to a desirable thickness. In an alternative embodiment, if a bulk substrate is used, an insulating material (e.g., oxide) may be used to electrically isolate subsequently formed components (e.g., fins).

In some embodiments, the base substrate **102** and the semiconductor layer **105** may include a same or similar semiconductor material. In other embodiments, the base substrate **102** and the semiconductor layer **105** may include a different material. The term "semiconductor material" as used herein may denote any semiconducting material including, for example, silicon (Si), germanium (Ge), silicon-germanium (SiGe) or other semiconductors. Multi-layers of semiconductor materials can also be used for the base substrate **102** and/or the semiconductor layer **105**. In an embodiment, both the base substrate **102** and the semiconductor layer **105** include silicon. In another embodiment, the base substrate **102** is a non-semiconductor material, such as, for example, a dielectric material and/or a conductive material.

The base substrate **102** and the semiconductor layer **105** may have similar or may have different crystal orientations. For example, the crystal orientation of the base substrate **102** and/or the semiconductor layer **105** may be {100}, {110}, or {111}. Other crystallographic orientations besides those specifically mentioned can also be used. The base substrate **102** and/or the semiconductor layer **105** may be a single crystalline semiconductor material, a polycrystalline material, or an amorphous material. Typically, at least the semiconductor layer **105** is a single crystalline semiconductor material. In some embodiments, the semiconductor layer **105**, located above the buried insulator layer **104**, can be processed to include semiconductor regions having different crystal orientations.

The buried insulator layer **104** may be a crystalline or non-crystalline oxide or nitride. In an embodiment, the buried insulator layer **104** is an oxide, such as, for example, silicon dioxide. The buried insulator layer **104** may be continuous or discontinuous. The buried insulator layer **104** may typically have a thickness from about 1 nm to about 500 nm. In an embodiment, the buried insulator layer **104** may have a thickness ranging from about 10 nm to about 100 nm. In an alternative embodiment, the buried insulator layer **104** may include multiple dielectric layers or a stack of dielectric layers including a silicon oxide layer and/or a silicon nitride layer.

With reference to FIG. **2**, the mandrels **106** may be formed in the semiconductor layer **105** using a hardmask **108**. The hardmask **108** may be formed on the semiconductor layer **105** using any deposition technique known in the art, such as, for example, chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, or physical vapor deposition. The hardmask **108** may include any masking material known in the art, such as, for example, silicon nitride (Si_3N_4), silicon carbide (SiC), silicon carbon nitride (SiCN), hydrogenated silicon carbide (SiCH), or any other masking material. In an embodiment, the hardmask **108** is a silicon nitride. A mandrel pattern may be formed in the hardmask **108** using any known patterning technique known in the art, such as, photolithography. The mandrels **106** may be formed by transferring the mandrel pattern into the semiconductor layer **105**. The mandrel pattern may be transferred into the semiconductor layer **105** by etching the semiconductor layer **105** selective to the hardmask **108** and the buried insulator layer **104** (i.e., etching the semiconductor layer **105**, where the hardmask **108** is a mask and the buried insulator layer **104** is an etch stop). There may be a mandrel pitch between any two adjacent mandrels. In an embodiment, a set of mandrels may be in a pFET region **101** and a set of mandrels may be in an nFET region **103**. It should be noted, a "set" may refer to any number of mandrels **106**, including a single mandrel. The mandrels **106** may have the same width as any adjacent mandrels.

Referring now to FIG. **3**, a demonstrative illustration of a structure **100** during an intermediate step of a method of fabricating III-V fins and IV fins having a similar fin pitch and on a shared surface is provided, according to an exemplary embodiment. More specifically, the method can include growing IV fins **110** on sidewalls of the mandrels **106**.