

Organization and Microprogramming, by Yao Yoahan Chu.

22. Firmware Computer

a. The following U.S. Pat. Nos. further disclose microprogrammed computer processors including microprogrammed control units with which the instant invention may be practiced:

3,400,371 issued 9/3/68;

3,656,123 issued 4/11/72.

What is claimed is:

1. In an internally programmed data processing apparatus having a memory comprised of a plurality of segments of addressable space, each segment being associated with a segment number for addressing said associated segment, each of said segments delineated by upper and lower variable bounds with predetermined ones of said segments storing a plurality of files of database record and at least one member database record, set of database records having at least one owner database record and at least one member database record, each of said database records having at least one pointer for linking predetermined ones of said database records to predetermined others of said database records and also to predetermined ones of said sets, each pointer comprised of an area, page and line address, said area address for locating a predetermined file of said database records, said page address for locating a predetermined group of said database records within said file, and said line address for locating a predetermined one of said database records, each of said database records also being associated with one each of a record descriptor for describing said associated database record, said record descriptors being stored in predetermined seconds of said segments, each of said sets also being associated with one each of a set-descriptor for describing said associated set and for providing a displacement address of said pointer in a first record of said set of associated records, said set descriptors being stored in predetermined thirds of said segments; said data processing apparatus further having a system base from which absolute addresses of said segments, database records and descriptors are referenced, said data processing apparatus also having a plurality of base registers, each base register for storing first coded electrical signals indicative of the segment number of any of said segments and also storing second coded electrical signals indicative of an offset address associated with the segment number, said offset address for addressing from the beginning of an associated segment any data within said associated segment; said data processing apparatus further having at least one index register for storing third coded electrical signals indicative of the area, page and line address of said predetermined one of said database records; said data processing apparatus further having an arithmetic and logic unit (ALU) having communication channels with said base registers, index registers and system base for performing arithmetic and logic operations of any data or address of said segments, database records, and descriptors;

instruction hardware responsive to fourth coded electrical signals indicative of a find owner instruction for finding the owner record (i.e. said predetermined one of said database records) of said predetermined first of said database records, said find owner instruction having a first base register address (BR) for identifying a first of said plurality

of base registers storing fifth coded electrical signals indicative of a first segmented address of said predetermined first of said database records, said first segmented address comprised of a first segment number in a first offset address of said predetermined first of said database records, and said find owner instruction further having a first address syllable for identifying a second of said base registers for providing a second segment number and second offset address of the set descriptor associated with said predetermined first of said database records, said instruction hardware comprising:

- a. first means coupled for being responsive to coded electrical signals stored in said first base register for fetching said fourth coded electrical signals indicative of said first segmented address into said arithmetic and logic unit;
- b. second means coupled to said first means for converting the fourth coded signals indicative of said first segmented address into seventh coded signals indicative of a first absolute address for locating said first of said database records relative to said system base;
- c. third means coupled to said second means for fetching eighth coded signals indicative of said first of said database records into said arithmetic and logic unit (ALU);
- d. fourth means coupled for being responsive to ninth coded signals indicative of said first address syllable for identifying said second of said base registers, said second base register storing tenth coded signals indicative of said second segment number and second offset address of said set descriptor associated with said predetermined first of said database records;
- e. fifth means coupled to said fourth means or converting said tenth coded signal indicative of said second number and second offset address into eleventh coded signals indicative of a second absolute address for locating said set descriptor associated with said predetermined first of said database records;
- f. sixth means coupled to said fifth means for fetching twelfth coded signals indicative of said set descriptor into said ALU;
- g. seventh means coupled for being responsive to thirteenth coded signals indicative of the displacement address in said set descriptor for addressing from the beginning of said first of said database records, an owner pointer of said pointers in said first of said database records; and,
- h. eighth means coupled to said seventh means for fetching fourteenth coded signals indicative of said owner pointer into said index register.

2. The apparatus as recited in claim 1 including ninth means coupled to said third coded signals in said index register for converting said third coded signals indicative of said area, page and line address of said predetermined one of said database records into fifteenth coded signals indicative of a third segmented address having a third segment number and third offset address for addressing said owner record (i.e. predetermined one of said database records).

3. The apparatus as recited in claim 2 coupled to said ninth means and said base registers and including tenth means for loading said fifteenth coded signals indicative of said third segmented address into said first base register.