US008673700B2

(12) **United States Patent**
Yedinak et al.

(10) **Patent No.: US 8,673,700 B2**
(45) **Date of Patent: Mar. 18, 2014**

(54) **SUPERJUNCTION STRUCTURES FOR POWER DEVICES AND METHODS OF MANUFACTURE**

(75) Inventors: **Joseph A. Yedinak**, Mountain Top, PA (US); **Mark L. Rinehimer**, Mountain Top, PA (US); **Praveen Muraleedharan Shenoy**, Kochi (IN)

(73) Assignee: **Fairchild Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 120 days.

(21) Appl. No.: **13/095,678**

(22) Filed: **Apr. 27, 2011**

(65) **Prior Publication Data**

US 2012/0276701 A1 Nov. 1, 2012

(51) **Int. Cl.**
H01L 21/00 (2006.01)
H01L 21/84 (2006.01)

(52) **U.S. Cl.**
USPC **438/156**; 438/141; 438/212; 257/302; 257/329; 257/341; 257/355; 257/E23.001; 257/E29.255

(58) **Field of Classification Search**
USPC 438/270, 133, 156, 212; 257/302, 341, 257/E23.001, E29.255
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,404,295 A 10/1968 Warner et al.
3,412,297 A 11/1968 Amlinger
3,497,777 A 2/1970 Teszner et al.
3,564,356 A 2/1971 Wilson
3,660,697 A 5/1972 Berglund et al.
4,003,072 A 1/1977 Matsushita et al.
4,300,150 A 11/1981 Colak
4,326,332 A 4/1982 Kenney et al.
4,337,474 A 6/1982 Yukimoto
4,345,265 A 8/1982 Blanchard
4,404,575 A 9/1983 Nishizawa
4,445,202 A 4/1984 Goetze et al.
4,579,621 A 4/1986 Hine
4,636,281 A 1/1987 Buiguez et al.
4,638,344 A 1/1987 Cardwell, Jr.
4,639,761 A 1/1987 Singer et al.
4,682,405 A 7/1987 Blanchard et al.
4,698,653 A 10/1987 Cardwell, Jr.

(Continued)

FOREIGN PATENT DOCUMENTS

CN 1036666 A 10/1989
CN 1744329 A 3/2006

(Continued)

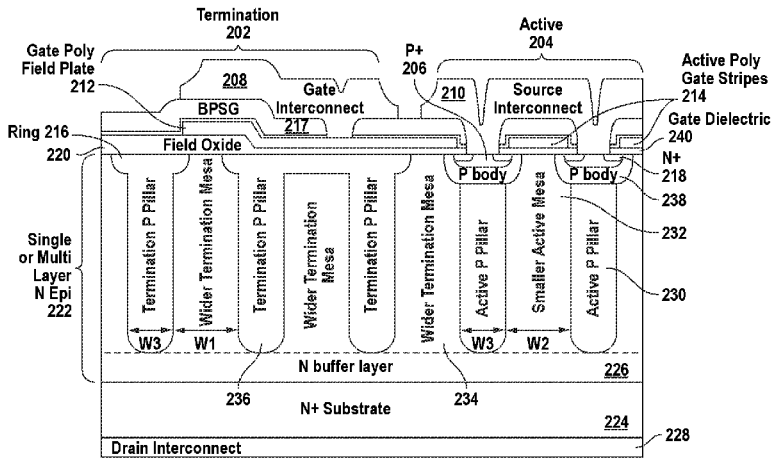
OTHER PUBLICATIONS

"CoolMOSä the second generation," Infineon Technologies product information, (2000), 2 pages total.

(Continued)

Primary Examiner — Lex Malsawma
Assistant Examiner — Eric Jones

(57) **ABSTRACT**

A power device includes a semiconductor region which in turn includes a plurality of alternately arranged pillars of first and second conductivity type. Each of the plurality of pillars of second conductivity type further includes a plurality of implant regions of the second conductivity type arranged on top of one another along the depth of pillars of second conductivity type, and a trench portion filled with semiconductor material of the second conductivity type directly above the plurality of implant regions of second conductivity type.

19 Claims, 54 Drawing Sheets